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8GB DDR4 SDRAM Datasheet

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Revision History

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Rev 1.1	2023/06	Official Release
Rev 1.2	2025/03	Updated Dimensions
Rev 1.3	2025/10	Updated Reset and Initialization Description

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1. Introduction

The 8Gb DDR4 SDRAM supports transfer rates up to 3200Mbps, suitable for general applications requiring high memory density and bandwidth. The chip is designed with key features of DDR4 SDRAM such as posted CAS, programmable CWL, internal (self) calibration, supports on-die termination, and asynchronous reset. All control and address inputs are synchronized with a pair of externally provided differential clocks. Inputs are latched at the crossing point of the differential clock (CK rising and CK falling). All I/Os are source-synchronized with a pair of bidirectional strobes (DQS_c and DQS_t).

2. Product List

Table 1 Package Information

Density	Configuration	Package	Part Number	Operating Temperature
8Gb	1G x 8	78-ball FBGA	YZ48G08V-F7HPI-M(0)	-40℃~85℃
			YZ48G08V-F7HPI-M	-55℃~105℃
8Gb	512M x 16	96-ball FBGA	YZ48G16V-F9HPI-M(0)	-40℃~85℃
			YZ48G16V-F9HPI-M	-55℃~105℃

3. Product Features

- VDD = VDDQ = 1.2V +/- 0.06V;
- VPP = 2.5V (2.375V~2.75V)
- 8Gb DDR4 SDRAM x8: 16 banks (4 bank groups) / 8Gb DDR4 SDRAM x16: 8 banks (2 bank groups)
- 8n prefetch architecture;
- Burst length of 8 (BL8) and burst chop of 4 (BC4);
- Bi-directional / differential data strobes;
- Supports dynamic on-die termination (ODT);
- Supports asynchronous reset;
- Supports ZQ calibration;
- Ensures CK-to-DQ and CK-to-DQS timing alignment via on-chip PLL;
- Supports programmable CAS latency (CL): 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22;
- Supports programmable additive latency of 0, CL-1, and CL-2;
- Programmable CAS write latency (CWL) = 12, 14 (DDR4-2400); 14, 18 (DDR4-2666); 16, 20 (DDR4-2933 and DDR4-3200);
- Average Refresh Cycle (when case temperature is 0° C ~ 95° C)

  7.8 μs at 0° C ~ 85° C

  3.9 μs at 85° C ~ 95° C
- JEDEC standard 78-ball FBGA (x8), 96-ball FBGA (x16);
- Supports DLL-off mode;
- Supports CA parity (Command/Address Parity) mode;
- Supports write CRC (Cyclic Redundancy Check) on data bus;
- Supports DBI (Data Bus Inversion);

- POD (Pseudo Open Drain) interface for data input/output;
- Internal VREF supply for data input;
- External VPP supply for DRAM activation;
- Supports PPR (Post-Package Repair) mode;
- Supports low-power self-refresh;
- Lead-free and RoHS compliant;
- JEDEC standard;

1. PPR mode is supported only in x16 configuration.
2. PPR mode is supported when Precharge All is issued.
3. TEN mode is supported only in x16 configuration.
4. TDQS mode is not supported in x8 configuration.

- Operating temperature: Industrial grade -I (-40° C ≤ Tc ≤ 95° C),Wide temperature grade -M (-55° C ≤ Tc ≤ 105° C)

3.1 Physical Characteristics

A. 78-ball FBGA (x8) package and dimensions;

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c				DM_n, DBI_n, TDQS_t	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	D
E	VSS	VDDQ	DQ6				DQ7	VDDQ	VSS	E
F	VDD	NC	ODT				CK_t	CK_c	VDD	F
G	VSS	NC	CKE				CS_n	NC	NC	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				NC	A13	VDD	N

1	2	3	4	5	6	7	8	9

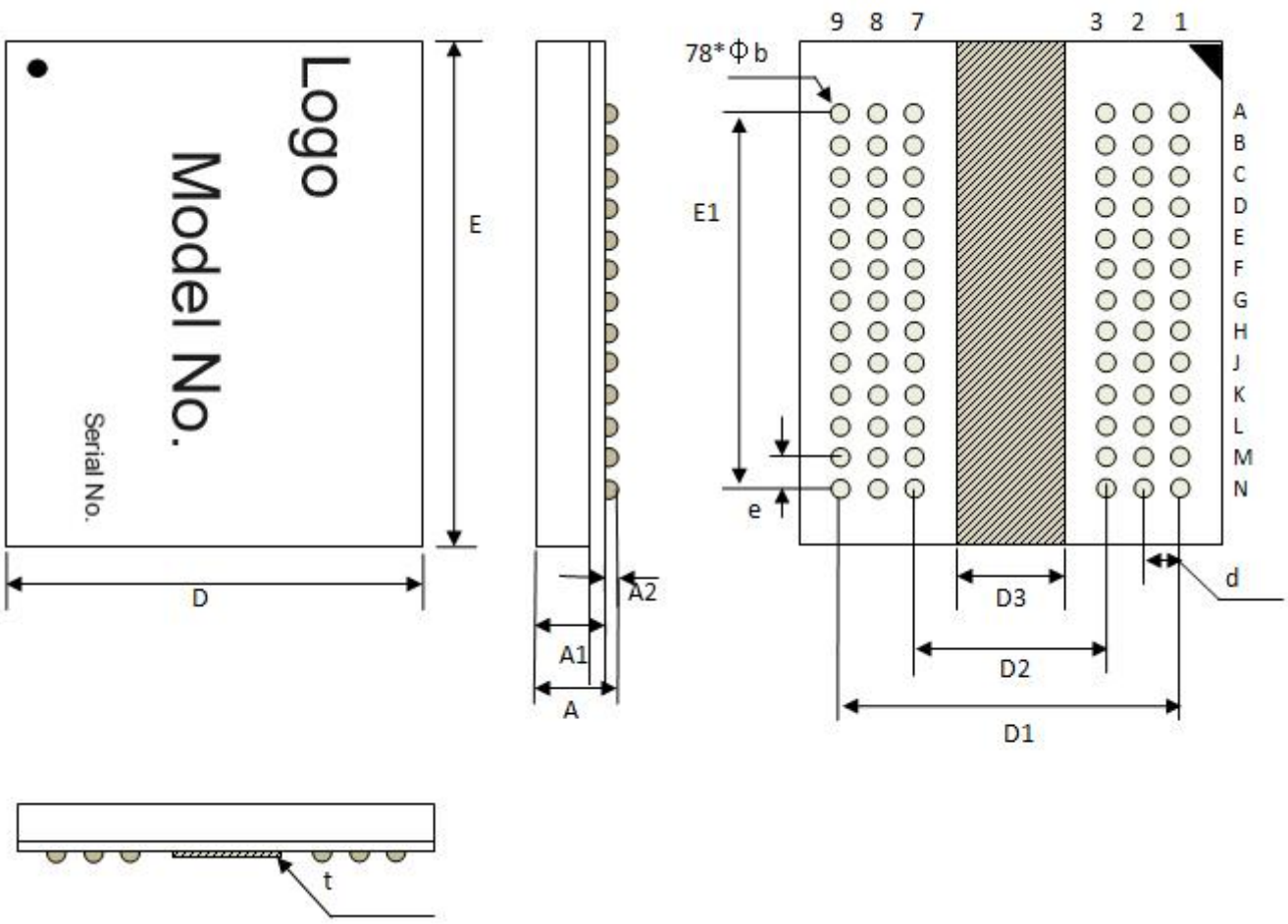


Figure 1 FBGA78 Package Drawing

Table 1 FBGA78 Dimension Drawing

Dimension Symbol	Main Dimension (mm)			Dimension Symbol	Main Dimension (mm)		
	Min	Nominal	Max		Min	Nominal	Max
A	—	1.12	1.20	D3	1.90	2.00	2.10
A1	0.73	0.78	0.83	t	0.142	0.155	0.168
A2	0.30	0.34	0.38	e	—	0.80	—
D	8.90	9.00	9.10	D1	6.30	6.40	6.50
E	13.90	14.00	14.10	E1	9.50	9.60	9.70
d	—	0.80	—	b	0.42	0.47	0.52

B. 96-ball FBGA (×16) Package and Dimensions;

	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQU0				DQSU_c	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	VSSQ	C
D	VDD	VSSQ	DQU6				DQU7	VSSQ	VDDQ	D
E	VSS	DMU_n/ DBIU_n	VSSQ				DML_n DBIL_n	VSSQ	VSS	E
F	VSSQ	VDDQ	DQSL_c				DQL1	VDDQ	ZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	VSS	VDDQ	G
H	VSSQ	DQL4	DQL2				DQL3	DQL5	VSSQ	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK_t	CK_c	VSS	K
L	VDD	WE_n/A14	ACT_n				CS_n	RAS_n/A16	VDD	L
M	VREFCA	BG0	A10/AP				A12/BC_n	CAS_n/A15	VSS	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	RESET_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T
	1	2	3	4	5	6	7	8	9	

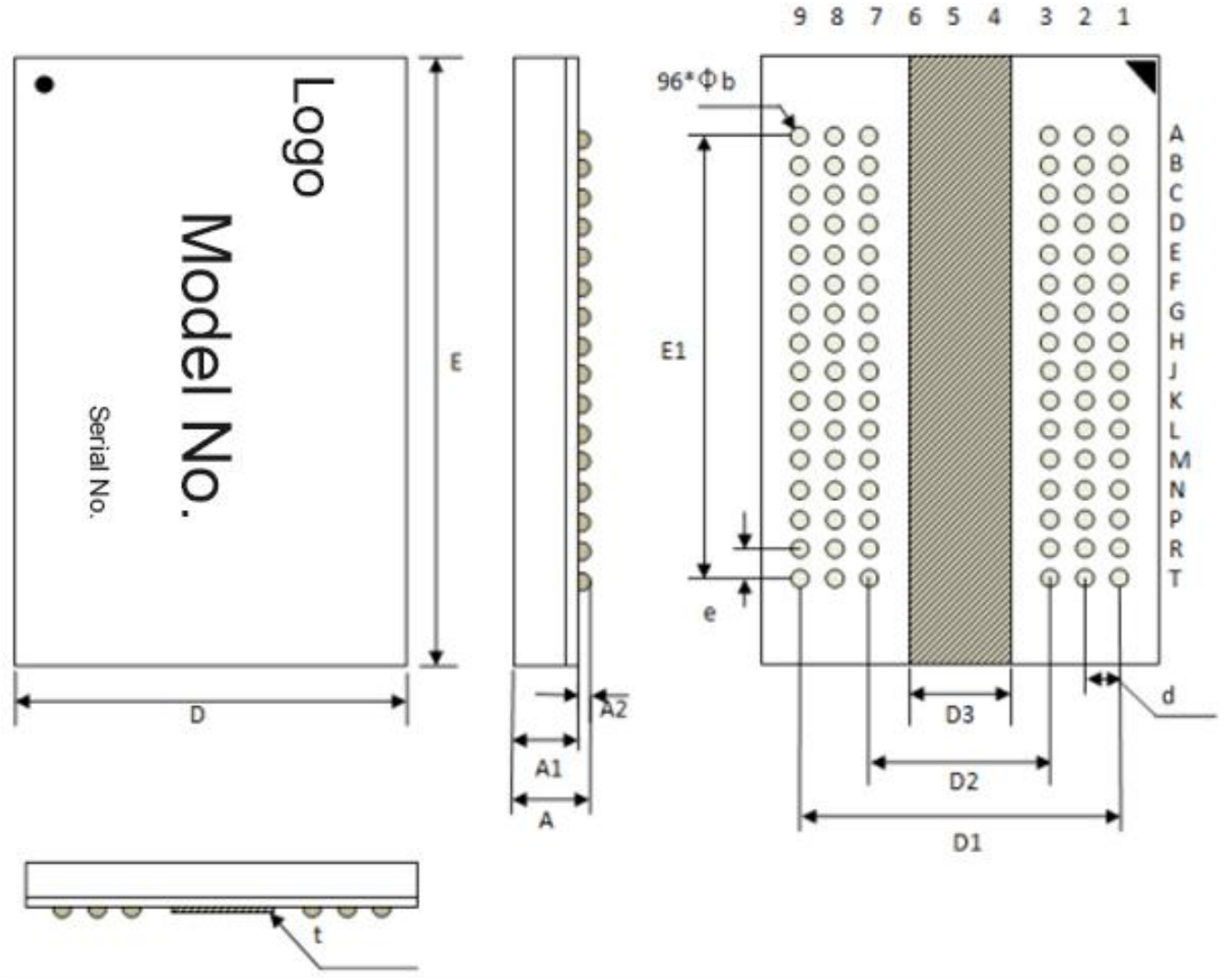


Figure 2 FBGA96 Package Drawing

Table 2 FBGA96 Dimension Drawing

Dimension Symbol	Main Dimension (mm)			Dimension Symbol	Main Dimension (mm)		
	Min	Nominal	Max		Min	Nominal	Max
A	—	1.12	1.20	D3	1.90	2.00	2.10
A1	0.73	0.78	0.83	t	0.142	0.155	0.168
A2	0.30	0.34	0.38	e	—	0.80	—
D	8.90	9.00	9.10	D1	6.30	6.40	6.50
E	13.90	14.00	14.10	E1	11.90	12.00	12.10
d	—	0.80	—	b	0.42	0.47	0.52

3.2 Pin Definitions

Table 1: DDR4 SDRAM Pin Descriptions

Symbol	Type	Function

CK_t, CK_c	Input	Clock Inputs: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled at the crossing of the positive edge of CK_t and the negative edge of CK_c. In connectivity test mode, clocks must be input differentially; MRS commands cannot be issued.
CKE	Input	Clock Enable: When CKE is high, it is active; when low, it is inactive. CKE controls the internal clock signals and the input and output buffers. When CKE is low, the device enters precharge power-down and self-refresh operation (all banks idle) or active power-down (any bank with an active row). CKE is used to synchronously exit self-refresh. VREFCA and internal DQ Vref must be maintained after stabilization during power-up and initialization and during all operations, including self-refresh. CKE must remain high during the entire read/write access. During power-down, input buffers other than CK_t, CK_c, ODT, and CKE are disabled. During self-refresh, input buffers (except CKE) are disabled.
CS_n	Input	Chip Select: When CS_n is set high, all commands are masked. CS_n provides external rank selection for systems with multiple ranks. CS_n is considered part of the command code.
ODT	Input	On-Die Termination signal: ODT (when set HIGH) enables RTT_NOM and controls the internal termination resistance of the DDR4 SDRAM. When enabled, for x8 configuration, ODT is applied only to each DQ, DQS_t, DQS_c, and DM_n/DBI_n/TDQS_t, NU/TDQS_c (when TDQS is enabled via mode register A11=1 in MR1) signals. For x16 configuration, ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signals. If MR1 is programmed to disable RTT_NOM, the ODT pin is ignored. When the ODT pin is active, RTT_NOM cannot be changed.
ACT_n	Input	Activate command input: ACT_n, together with CS_n, defines the activate command input. When data is input to RAS_n/A16, CAS_n/A15, and WE_n/A14, these pins are considered row address A16, A15, and A14.

RAS_n/A16 **CAS_n/A15** **WE_n/A14**	Input	Command input: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) are used to define the input commands. These pins have multiple functions. For example, when ACT_n is LOW (active), these pins serve as addresses A16, A15, and A14; when ACT_n is HIGH (inactive), these pins serve as command inputs. Refer to the Command Truth Table for specific functions to determine Read, Write, and other commands.
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is the input mask signal for write data. During a write access, when DM_n is sampled LOW, the input data is masked. DM_n is sampled on both rising and falling edges of DQS. DM is enabled via mode register bits A10, A11, A12 in MR5 and shares the function with DBI. For x8 devices, DM or TDQS function is enabled via mode register bit A11 in MR1. DBI_n is an input/output signal that indicates whether the stored/output data is true or inverted. If DBI_n is LOW, the data is inverted before storage/output inside the DDR4 SDRAM; if DBI_n is HIGH, no inversion occurs. TDQS is supported only in x8 devices.
BG0 – BG1	Input	Bank Group input: BG0 – BG1 define which bank group is being targeted for Activate, Read, Write, or Precharge commands. BG0 also determines which mode register is accessed during an MRS cycle. x4/8 have BG0 and BG1, but x16 has only BG0.
BA0 – BA1	Input	Bank address input: BA0 – BA1 define the bank to which the Activate, Read, Write, or Precharge command is being applied. The bank address also determines which mode register is accessed during an MRS cycle.
A0 – A16	Input	Address inputs: Provide row address for ACTIVATE commands, and column address for read/write commands to select a location from the memory array of the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15, WE_n/A14 have additional functions.) Address inputs also provide the op-code during mode register set commands.

A10 / AP	Input	Auto precharge: A10 is sampled during read/write commands to determine whether auto precharge will be performed on the accessed bank after the read/write operation. (High: auto precharge; Low: no auto precharge). A10 is sampled during the precharge command to determine whether the precharge applies to one bank (A10 Low) or all banks (A10 High). If only one bank is to be precharged, the bank is selected by the bank address.
A12 / BC_n	Input	Burst chop: A12 / BC_n is sampled during read/write commands to determine whether burst chop (on-the-fly) will be performed. (High: no burst chop; Low: burst chop). Refer to the command truth table for details.
RESET_n	Input	Active low asynchronous reset: Reset when RESET_n is Low, and no reset when RESET_n is High. Under normal operation, RESET_n must be at High. RESET_n is a CMOS rail-to-rail signal with DC high and low levels at 80% and 20% of VDD, respectively.
DQ	Input/Output	Data input/output: Bidirectional data bus. If CRC is enabled via the mode register, the CRC code is appended at the end of the data burst. During test, by setting MR4 A4=1 via the mode register, any DQ from DQ0~DQ3 can indicate the internal Vref level. In this mode, RTT should be set to Hi-Z. Refer to the vendor-specific data sheet to determine which DQ to use.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/Output	Data strobe: Output with read data, input with write data. Edge-aligned with read data, center-aligned with write data. For x16, DQSL corresponds to data on DQL0-DQL7; DQSU corresponds to data on DQU0-DQU7. Data strobes DQS_t, DQSL_t, and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c respectively to provide differential pair signals to the system during read and write. DDR4 SDRAM supports only differential data strobes, not single-ended.
TDQS_t, TDQS_c	Output	Terminal Data Strobe: TDQS_t/TDQS_c are only applicable for x8 DRAM. When enabled by Mode Register A11 = 1 in MR1, the DRAM enables the same termination resistor function for TDQS_t/TDQS_c as applied to DQS_t/DQS_c. When disabled by Mode Register A11 = 0 in MR1, DM/DBI/TDQS provides Data Mask function or Data Bus Inversion function according to MR5; A11, A12, A10 and TDQS_c are not used.

		x4/x16 DRAM must disable the TDQS function by Mode Register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input: DDR4 supports even parity in the DRAM with MR settings. Once enabled via the register in MR5, the DRAM calculates parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. When the command is latched on the rising edge of CK_t and CS_n is LOW, the command and address inputs must perform parity check.
ALERT_n	Input/Output	Alert signal: It has multiple functions such as CRC error flag, command and address parity error flag as output signals. If there is an error in CRC, Alert_n goes LOW for a time interval and then returns HIGH. If there is an error in command address parity, Alert_n goes LOW for a relatively long time until the ongoing internal DRAM recovery transaction completes. In connectivity test mode, this pin acts as an input. Whether to use this signal depends on the system. If not connected as a signal, the ALERT_n pin must be tied to VDD on the board.
TEN	Input	Connectivity Test Mode Enable: Required on x16 devices, not supported on x4/x8. This pin HIGH will enable connectivity test mode to operate with other pins. It is a CMOS rail-to-rail signal with AC high and low levels at 80% and 20% of VDD respectively. Whether to use this signal depends on the system. This pin is internally pulled down to VSS via a weak pull-down resistor.
NC		No Connect: No internal electrical connection.
VDDQ	Power Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Power Supply	DQ Ground
VDD	Power Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Power Supply	Ground
VPP	Power Supply	Activation Voltage: 2.5V (2.375V min, 2.75V max)
VREFCA	Power Supply	CA Reference Voltage
ZQ	Power Supply	ZQ Calibration Reference Pin

4. 8Gb DDR4 DRAM Addresses

Table 2: 8Gb DDR4 SDRAM Addresses

Configuration		1G x 8	512 M x 16
Bank Address	# of Bank Groups	4	2
	BG Address	BG0~BG1	BG0
	Bank Address within a BG	BA0~BA1	BA0~BA1
Row Address		A0~A15	A0~A15
Column Address		A0~A9	A0~A9
Page		1KB	2KB

5. State Diagram

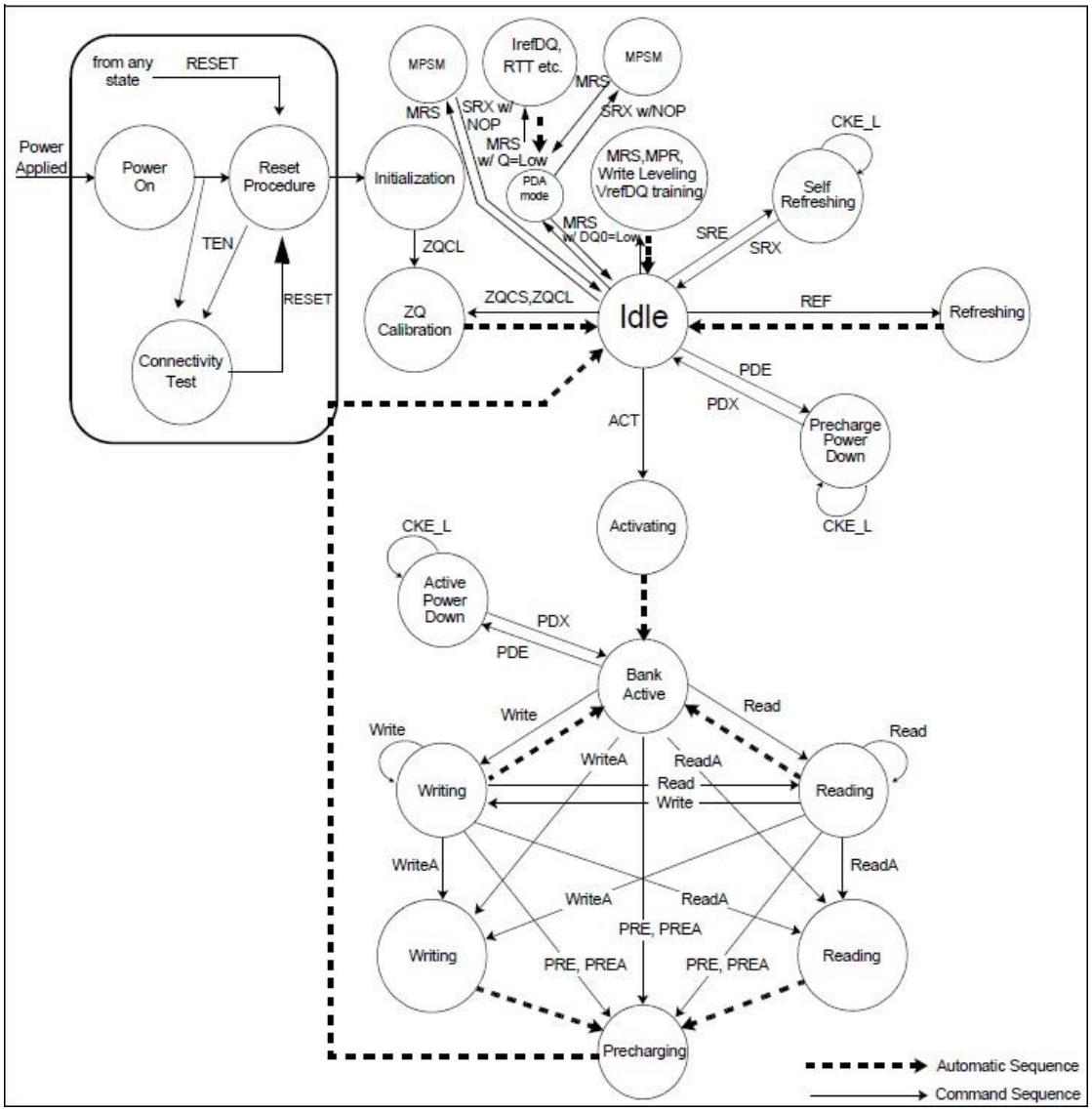


Figure 1 Chip Functional Block Diagram

Table 3 State Diagram Command Definition

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	PRECHARGE All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh exit
REF	Refresh, Fine granularity Refresh	RESET_n	Start RESET procedure	MPR	Multi Purpose Register
TEN	Boundary Scan Mode Enable				

6. Basic Functions

DDR4 SDRAM is a high-speed dynamic random access memory. The x8 configuration is internally organized as 16 banks, divided into 4 bank groups of 4 banks each; the x16 configuration is 8 banks, divided into 2 bank groups of 4 banks each. DDR4 SDRAM uses an 8n prefetch architecture to achieve high-speed operation. This architecture is combined with an interface that transfers two data words per clock cycle at the I/O pins. A single read or write operation for DDR4 SDRAM consists of a single 8n-bit wide, 4-clock-cycle data transfer at the internal DRAM core and 8 corresponding n-bit wide, 4-clock-cycle data transfers at the I/O pins.

Read and write accesses to the DDR4 SDRAM are burst oriented; they start at a selected location and continue for a burst length of 8 or a burst length of 4 in a programmed sequence. The operation begins with the registration of an ACTIVATE command, followed by a Read or Write command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bank group; BA0-BA1 select the bank; A0-A17 select the row; see "DDR4 SDRAM Addressing" for details). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine whether to issue an auto precharge command (via A10, if enabled in the mode register), and select BC4 or BL8 mode (via A12, on-the-fly).

Before normal operation, the DDR4 SDRAM must be powered up and initialized in a predetermined manner.

The following sections provide detailed information including device reset and initialization, register definitions, command descriptions, and device operation.

6.1 Reset and Initialization

For power-up and reset initialization, the following default settings for MR (Mode Register) are required to prevent

improper DRAM function.

Gear down mode (MR3 A[3]): 0 = 1/2 Rate

Per DRAM Addressability (MR3 A[4]): 0 = Disabled

Max Power Saving Mode (MR4 A[1]): 0 = Disabled

CS to Command/Address Latency (MR4 A[8:6]): 000 = Disabled

CA Parity Latency Mode (MR5 A[2:0]): 000 = Disabled

Hard Post Package Repair mode (MR4 A[13]): 0 = Disabled

Soft Post Package Repair mode (MR4 A[5]): 0 = Disabled

6.1.1 Power-Up Initialization Sequence

The power-up and initialization sequence requires the following order:

1. Apply power (it is recommended that RESET_n and TEN be kept below 0.2 × VDD; all other inputs may be undefined). After the power supply stabilizes, RESET_n must be kept below 0.2 × VDD for at least 200 µs; after the power supply stabilizes, TEN must be kept below 0.2 × VDD for at least 700 µs. Before de-asserting RESET_n, CKE must be pulled LOW (minimum time of 10 ns). The rise time of the power supply voltage from 300 mV to VDD min must not exceed 200 ms; during the rise, VDD ≥ VDDQ and (VDD - VDDQ) < 0.3 V. VPP must ramp simultaneously with or earlier than VDD, and VPP must always be equal to or higher than VDD.

- VDD and VDDQ are driven by a single power supply
- Voltage levels on all pins except VDD, VDDQ, VSS, and VSSQ must not exceed VDD and VDDQ, and must not be lower than VSS and VSSQ. Additionally, after the power supply voltage rise is complete, VTT voltage must be at most 0.66 V.
- VrefCA = VDD/2.

or

- Apply VDD before or at the same time as VDDQ, without any slope reversal.
- Apply VDDQ before or at the same time as VTT and VrefCA, without any slope reversal.
- Apply VPP before or at the same time as VDD, without any slope reversal.
- Voltage levels on all pins except VDD, VDDQ, VSS, and VSSQ must be less than or equal to VDDQ and VDD, and must be greater than or equal to VSSQ and VSS.

2. After RESET# is de-asserted, wait 500 µs before CKE becomes active. During this time, the DRAM will begin internal state initialization; this is done independently of the external clock.

3. Before CKE is activated, the clocks (CK, CK#) must be started and stable for at least 10 ns or 5 tCK (whichever is greater). Since CKE is a synchronous signal, the corresponding clock setup time (tIS) must be met. Additionally,

a deselect command must be registered at clock edge Td (with tIS setting the clock timing). Once CKE is registered HIGH after reset, CKE must remain HIGH until the initialization sequence is complete, including the end of tDLLK and tZQinit.

4. While RESET# is asserted, the DDR4 DRAM will keep its pin terminations in a high-impedance state. Additionally, after RESET# is de-asserted, the DRAM remains in a high-impedance state until CKE becomes HIGH. Before CKE goes HIGH, the ODT input signal may be in a high-impedance or indeterminate state. When CKE goes HIGH, the ODT input signal can be statically held at HIGH or LOW. If RTT_NOM is enabled in register MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power-up initialization sequence is complete, including the end of tDLLK and tZQinit.

5. After CKE is registered HIGH, wait for the minimum reset CKE exit time tXPR before issuing the first MRS command to load the mode register. [tXPR = max(tXS, 5 tCK)].

6. Issue an MRS command to load all application configurations into register MR3. (Ensure that the MRS command configures register MR3 with BG0 LOW, and BA1 and BA0 HIGH.)

7. Issue an MRS command to load all application configurations into register MR6. (Ensure that the MRS command configures register MR6 with BA0 LOW, and BA1 and BG0 HIGH.)

8. Issue an MRS command to load all application configurations into register MR5. (Ensure that the MRS command configures register MR5 with BA0 HIGH, BA1 LOW, and BG0 HIGH.)

9. Issue MRS command to load all application configurations into register MR4. (Ensure that when issuing MRS command to configure register MR4, BA1, BA0 are set low, BG0 is set high.)

10. Issue MRS command to load all application configurations into register MR2. (Ensure that when issuing MRS command to configure register MR2, BA0, BG0 are set low, BA1 is set high.)

11. Issue MRS command to load all application configurations into register MR1. (Ensure that when issuing MRS command to configure register MR1, BA1, BG0 are set low, BA0 is set high.)

12. Issue MRS command to load all application configurations into register MR0. (Ensure that when issuing MRS command to configure register MR0, BA1, BG0, BA0 are all set low.)

13. Issue ZQCL command to start ZQ calibration.

14. Wait for tDLLK and tZQinit to complete.

15. DDR4 SDRAM is now ready for read/write training (including Vref training and write leveling).

6.1.2 VDD Slew Rate during Power-Up Initialization Sequence

Table 4 VDD Slew Rate

Symbol	Min	Max	Unit
VDD sla	0.004	600	V/ms[b]
VDD_on[a]	TBD	200	ms[c]

Note:

a. Measurement is performed between 300 mV and 80% VDD.

b. Bandwidth measurement is limited to 20 MHz.

C. The maximum time for VDD to ramp from 300 mV to VDD minimum is [value].

6.1.3 Reset Initialization after Power Stable

Initializing RESET without power interruption requires the following sequence:

1. When a reset is needed, pull RESET_n low to below 0.2 × VDD (all other inputs may be undefined). RESET_n must remain low for at least tPW_RESET. Before RESET_n is released low, CKE must remain low for at least 10 ns.

2. Perform steps 2 through 10 of Section 6.1.1 "Power-Up Initialization Sequence".

3. The reset sequence is complete; the DDR4 SDRAM is ready for read/write training (including Vref training and write leveling).

6.2 Mode Registers

MR0 Mode Register

Address	Operating Mode	Description
BG1	RFU	0 = Must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = Must be programmed to 0 during MRS
A12, A11, A10, A9	WR and RTP[2,3]	Write Recovery and Read to Precharge (RTP) (See Table 5)
A8	DLL Reset	0 = No Reset 1 = Reset
A7	TM	0 = Normal 1 = Test
A12, A6:A4, A2	CAS Latency	(See Table 6)
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1:A0	Burst Length	00 = 8 (Fixed) Abbrev. BL8MRS 01 = BC4 or 8 (on the fly) Abbrev. BC4OTF or BL8OTF 10 = BC4 (Fixed) Abbrev. BC4MRS 11 = Reserved

Note:

1. When BG0, BA1, BA0 = 111, the register control word setting is Reserved. The DRAM ignores the MR command and does not respond. When the RFU MR Code is set as input, the DRAM operation is undefined.

2. The minimum WR (write recovery for auto precharge) within a clock cycle is calculated based on the rounding algorithm defined in Section 14.5. The WR value in the mode register must be programmed to be equal to or greater than WRmin. The programmed WR value, together with tRP, determines tDAL.

3. The table provides the encoding for write recovery and internal read command to precharge command delay. Refer to the AC timing table for actual write recovery time.

4. This table shows only the encoding for a given CAS latency. For actual supported CAS latencies, refer to the speed bin table for each frequency. CAS latency controlled by A12 is optional for 4Gb devices.

5. The WR and RTP settings from A13 are optional for 4Gb devices.

Table 5: Write Recovery and Read Precharge (Cycles)

A13	A11	A10	A9	WR	RTP
0	0	0	0	10	5
0	0	0	1	12	6
0	0	1	0	14	7
0	0	1	1	16	8
0	1	0	0	18	9
0	1	0	1	20	10
0	1	1	0	24	12
0	1	1	1	22	11
1	0	0	0	26	13
1	0	0	1	Reserved	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved
1	1	0	0	Reserved	Reserved
1	1	0	1	Reserved	Reserved
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

Table 6 CAS Latency

A12	A6	A5	A4	A2	CAS latency
0	0	0	0	0	9
0	0	0	0	1	10

0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	18
0	1	0	0	1	20
0	1	0	1	0	22
0	1	0	1	1	24
0	1	1	0	0	23
0	1	1	0	1	17
0	1	1	1	0	19
0	1	1	1	1	21
1	0	0	0	0	Reserved
1	0	0	0	1	26
1	0	0	1	0	Reserved
1	0	0	1	1	28
1	0	1	0	0	Reserved
1	0	1	0	1	30
1	0	1	1	0	Reserved
1	0	1	1	1	32
1	1	0	0	0	Reserved

MR1 Mode Register

Address	Operating Mode	Description
BG1	RFU	0 = Must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[3]
A17	RFU	0 = Must be programmed to 0 during MRS
A13	RFU	0 = Must be programmed to 0 during MRS
A12	Qoff[1]	0 = Output Buffer Enable 1 = Output Buffer Disable
A11	TDQS enable	0 = Disable 1 = Enable

A10, A9, A8	RTT_NOM	(See Table 7)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A6, A5	RFU	0 = Must be programmed to 0 during MRS
00 = 0 (AL Disable), 01 = CL-1, 10 = CL-2, 11 = Reserved	Additive Latency	00 = 0 (AL Disable) 10 = CL-2 01 = CL-1 11 = Reserved
A2, A1	Output Driver Impedance Control	(See Table 8)
A0	0 = Disable, 1 = Enable	0 = Disable 1 = Enable

Note:

1. Output disable: DQS, DQS_t, DQS_c;

2. In DDR4, output disable polarity: 1 = disable, 0 = enable.

3. Reserved for register control word setting. When BG0, BA1, BA0=111, the DRAM ignores the MR command and does not respond. When RFU MR code is set as input, DRAM operation is undefined.

Table 7 RTT_NOM

A10	A9	A8	RTT_NOM
0	0	0	RTT_NOM disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

Table 8 Output Driver Impedance Control

A2	A1	RTT_NOM
0	0	RZQ/7
0	1	RZQ/5
1	0	Reserved
1	1	Reserved

MR2 Mode Register

Address	Operating Mode	Descriptio n
BG1	RFU	0 = Must be programmed to 0 during MRS

BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = Must be programmed to 0 during MRS
A13	RFU	0 = Must be programmed to 0 during MRS
A12	0 = Disable, 1 = Enable	0 = Disable 1 = Enable23
A11, A10:A9	RTT_WR	(See Table 9)
A8, A2	RFU	0 = Must be programmed to 0 during MRS
A7:A6	Low Power Auto Self Refresh(LPASR)	00 = Manual Mode (Normal Operating Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self-Refresh)
A5:A3	CAS Write Latency (CWL)	(see Table 10)
A1:A0	RFU	0 = Must be programmed to 0 during MRS

Note:

1. Reserved for register control word setting. When BG0, BA1; BA0=111, the DRAM ignores the MR command and does not respond. When the RFU MR Code is set as input, the DRAM operation is undefined.

2. After a WCRC error occurs, the user can read the CRC error status information using MPR. However, for the next WCRC error to be recorded in the MPR, a write operation without a WCRC error must be initiated. Otherwise, even inserting the CRC error Clear configured via MRS will not take effect.

3. For x16, when the DRAM detects an error in the CRC tree, the DDR4 DRAM will mask all DQ.

Table 9 RTT_WR

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT Off
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Table 10 CWL (CAS Write Latency)

A5	A4	A3	CWL	Operating Data Rate MT/s 1 tCK Write Preamble	Operating Data Rate MT/s 2 tCK Write Preamble 1

				1st set	2nd set	1st set	2nd set
0	0	0	9	1600			
0	0	1	10	1866			
0	1	0	11	2133	1600		
0	1	1	12	2400	1866		
1	0	0	14	2666	2133	2400	
1	0	1	16	2933 / 3200	2400	2666	2400
1	1	0	18		2666	2933 / 3200	2666
1	1	1	20		2933 / 3200		2933 / 3200

Note: 2 tCK write preamble is valid for DDR4-2400/2666/2933/3200 speed grades. For the second set of 2 tCK write preamble, no additional CWL is required.

MR3 Mode Register

Address	Operating Mode	Description
BG1	RFU	0 = Must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = Must be programmed to 0 during MRS
A13	RFU	0 = Must be programmed to 0 during MRS
A12:A11	MPR Read Format	0 = Serial 10 = Interleaved 01 = Parallel 11 = Reserved
A10:A9	Write CMD Latency when CRC and DM are enabled	(see Table 12)
A8:A6	Fine Granularity Refresh Mode	(see Table 11)
A5	Temperature sensor readout	0 = Disable 1 = Enable
A4	Per DRAM Addressability	0 = Disabled 1 = Enabled
A3	Geardown Mode	0 = 1/2 Rate 1 = 1/4 Rate
A2	MPR Operation	0 = Normal 1 = Data flow from/to MPR

A1:A0	MPR Page Selection (see Table 13)	00 = Page0 01 = Page1	10 = Page2 11 = Page3

Note:

1. Reserved for register control word setting. When BG0, BA1; BA0=111, the DRAM ignores the MR command and does not respond. When the RFU MR Code is set as input, the DRAM operation is undefined.

2. If entering PDA mode, MRS is configured for Burst Length OTF mode (MR0[1:0]=0b01). After exiting PDA, the SOC should reconfigure for Burst Length OTF mode (MR0[1:0]=0b01).

Table 11 Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on-the-fly 2x
1	1	0	Enable on-the-fly 4x
1	1	1	Reserved

Table 12: Write Command Delay Time When CRC and DM Are Both Enabled, MR3 A[10:9]

A10	A9	CRC+DM Write Command Latency	Operating Data Rate
0	0	4nCK	1600
0	1	5nCK	1866, 2133, 2400, 2666
1	0	6nCK	2933, 3200
1	1	RFU	RFU

Table 13: MPR Data Format

MPR Page 0 (Training Mode)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (Default Value)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

MPR Page 1 (CA Parity Error Log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note

BA1:BA0	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Read Only
	01 = MPR1	CAS_n/A15	WE_n/A14	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]	
	10 = MPR2	PAR	ACT_n	BG[1]	BG[0]	BA[1]	BA[0]	A[17]	RAS_n/A16	
	11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Delay 4			C[2]	C[1]	C[0]	
				MR5. A[2]	MR5. A[1]	MR5. A[0]				

Note:

1. Enable MPR for CA parity error log readout by setting A[2] in MR3.

2. For 8Gb DDR4, A[17] is not used; MPR2[1] should be considered a 'Don't Care'.

3. If used in a single-die application where C[2:0] are not used, then MPR3[2:0] should be considered 'Don't Care'.

4. MPR3 bits 0-2 (CA parity latency) reflect the latest programmed CA parity latency value.

MPR Page 2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	hPPR	sPPR	RTT_WR	Temperature Sensor Status		CRC CRC Write Enable	Rtt_WR		Read Only
		–	–	MR2	–	–	MR2	MR2		
				A11	–	–	A12	A10	A9	
	01 = MPR1	Vref DQ Tmg Range	Vref DQ training value						Speed down enable	
		MR6	MR6						MR3	
		A6	A5	A4	A3	A2	A1	A0	A3	
	10 = MPR2	CAS latency					CAS write latency			
		MR0					MR2			
		A6	A5	A4	A2	A12	A5	A4	A3	
	11 = MPR3	Rtt_Nom			Rtt_Park			Driver resistance		
		MR1			MR5			MR1		
		A10	A9	A6	A8	A7	A6	A2	A1	

Note:

1. MR bit for temperature sensor readout.

2. MR3 bit A5 = 1: DRAM updates the temperature sensor status in MPR Page2 (MPR0 bits A4:A3). The temperature data is guaranteed to be updated within 32 ms when the MPR reads the temperature sensor status bit.

3. MR3 bit A5 = 0: DRAM disables update of temperature sensor status in MPR Page2 (MPR0 bits A4:A3)

MPR0 bit A4	MPR0 bit A3	Refresh rate speed range
0	0	Sub 1X refresh (> tREFI)
0	1	1X refresh rate (= tREFI)
1	0	2X refresh rate (1/2*tREFI)
1	1	Reserved

MPR page3 (Supplier use only)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1:BA0	00 = MPR0	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored	Read Only
	01 = MPR1	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored	
	10 = MPR2	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored	Ignored	
	11 = MPR3	Ignored	Ignored	Ignored	Ignored	MAC	MAC	MAC	MAC	

MR4 Mode Register

Address	Operating Mode	Description
BG1	RFU	0 = Must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW1
A17	RFU	0 = Must be programmed to 0 during MRS
A13	hPPR	0 = Disabled 1 = Enabled
A12	Write Preamble	0 = 1 nCK 1 = 2 nCK
A11	Read Preamble	0 = 1 nCK 1 = 2 nCK
A10	Read Preamble Training Mode	0 = Disabled 1 = Enabled
A9	Self-Refresh Termination	0 = Disabled 1 = Enabled

A8:A6	CS to CMD/ADDR Delay Mode (cycles)	000 = Disabled 100 = 6 001 = 3 101 = 8 010 = 4 110 = Reserved 011 = 5 111 = Reserved (see Table 14)
A5	sPPR	0 = Disabled 1 = Enabled
A4	Internal Vref Monitor	0 = Disabled 1 = Enabled
A3	Temperature Controlled Refresh Mode	0 = Disabled 1 = Enabled
A2	Temperature Controlled Refresh Range	0 = Normal 1 = Extended
A1	Maximum Power-Down 1	0 = Disabled 1 = Enabled
A0	RFU	0 = Must be programmed to 0 during MRS

Note

1. Reserved for register control word setting. When BG0, BA1; BA0=111, the DRAM ignores the MR command and does not respond. When the RFU MR Code is set as input, the DRAM operation is undefined.

2. When exiting Maximum Power-Down mode, the DLL must be reset or a full initialization procedure must be completed in the system.

Table 14 CS to CMD/ADDR Delay Mode Settings

A8	A7	A6	CAL
0	0	0	Disabled
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

MR5 Mode Register

Address	Operating Mode	Description
BG1	RFU	0 = Must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = Must be programmed to 0 during MRS
A13	RFU	0 = Must be programmed to 0 during MRS

A12	Read DBI	0 = Disable	1 = Enable
A11	Write DBI	0 = Disable	1 = Enable
A10	Data Mask	0 = Disable	1 = Enable
A9	CA Parity Persistent Error	0 = Disable	1 = Enable
A8:A6	RTT_PARK	(see Table 15)	
A5	Power-Down Mode ODT Input Buffer	0 = ODT input buffer enabled 1 = ODT input buffer disabled	
A4	CA Parity Error Status	0 = Clear	1 = Error
A3	CRC Error Status Clear	0 = Clear	1 = Error
A2:A0	CA Parity Latency Mode	(see Table 16)	

Note

1. Reserved for register control word setting. When BG0, BA1; BA0=111, the DRAM ignores the MR command and does not respond. When the RFU MR Code is set as input, the DRAM operation is undefined.

2. When RTT_NOM is disabled in MR1, A5 in MR5 is ignored.

Table 15 – RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

Table 16 – C/A Parity Latency Mode

A2	A1	A0	PL	Speed Bin
0	0	0	Disabled	
0	0	1	4	1600, 1866, 2133
0	1	0	5	2400, 2666
0	1	1	6	2933, 3200
1	0	0	8	RFU
1	0	1	Reserved	

1	1	0	Reserved	
1	1	1	Reserved	

Note: Parity latency must be programmed according to the timing parameters in the speed bin table.

MR6 Mode Register

Address	Operating Mode	Description
BG1	RFU	0 = Must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = Must be programmed to 0 during MRS
A13	RFU	0 = Must be programmed to 0 during MRS
A12:A10	tCCD_L	(See Table 17)
A9,A8	RFU	0 = Must be programmed to 0 during MRS
A7	VrefDQ Training Enable	0 = Disable (Normal Operating Mode) 1 = Enable (Training Mode)
A6	VrefDQ Training Range	(See Table 18)
A5:A0	VrefDQ Training Value	(See Table 19)

Note

1. Reserved for register control word settings. When BG0, BA1; BA0=111, the DRAM ignores the MR command and does not respond.

Table 17 tCCD_L and tDLLK

A12	A11	A10	tCCD_L.min(nCK)1	tDLL_K.min(nCK)1	Note
0	0	0	4	597	Data rate ≤ 1333Mbps
0	0	1	5		1333Mbps < Data rate ≤ 1866Mbps (1600/1866Mbps)
0	1	0	6	768	1866Mbps < Data rate ≤ 2400Mbps

					(2133/2400Mbps)
0	1	1	7	1024	2400Mbps < Data rate ≤ 2666Mbps (2666Mbps)
1	0	0	8		2666Mbps < Data rate ≤ 3200Mbps (2933/3200Mbps)
1	0	1	Reserved		
1	1	0			
1	1	1			

Note: tCCD_L/tDLLK should be programmed according to the values defined in the AC parameters table for each operating frequency.

Table 18 VrefDQ Training: Range

A6	VrefDQ Range
0	Range 1
1	Range 2

Table 19 VrefDQ Training: Values

A5:A0	**Range 1**	**Range 2**	**A5:A0**	**Range 1**	**Range 2**
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	66.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%

01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 111111	Reserved	Reserved

MR7 DRAM: Ignore

For all DDR4 SDRAM, any access to MR7 can be ignored. In DDR4 SDRAM, any bit within MR7 may be set to invalid.

6.3 Per DRAM Addressability

DDR4 allows programmability for a given device on a rank. For example, this feature can be used to program different ODT or Vref values on the DRAMs of a given rank.

2. Write leveling must be performed before entering Per DRAM Addressability (PDA) mode;

3. Before entering Per DRAM Addressability (PDA) mode, the following mode register settings can be performed: - RTT_PARK MR5 {A8:A6} = Enable - RTT_NOM MR1 {A10:A9:A8} = Enable;

4. Enable Per DRAM Addressability (PDA) mode using MR3 bit "A4=1";

5. In Per DRAM Addressability mode, all MRS commands use DQ0 for x4 and x8, and DQ0 for x16 as a qualifier. The DRAM captures DQ0 for x4 and x8 using DQS_c and DQS_t, and DQ0 for x16 using DQSL_c and DQSL_t, as shown in Figure 2. If DQ0 is 0 for x4 and x8, and DQ0 is 0 for x16, the DRAM executes the MRS command. If DQ0 is 1, the DRAM ignores the MRS command. The controller can choose to drive all DQ bits.

6. Program the desired device and mode registers using MRS commands, using DQ0 for x4 and x8, and DQ0 for x16.

7. In Per DRAM Addressability mode, only MRS commands are allowed.

8. In PDA mode, the mode register set command cycle time AL + CWL + BL/2 - 0.5tCK + tMRD_PDA + (PL) is the time required to complete the write to the mode register, and is also the minimum time required between two MRS commands as shown in Figure 2.

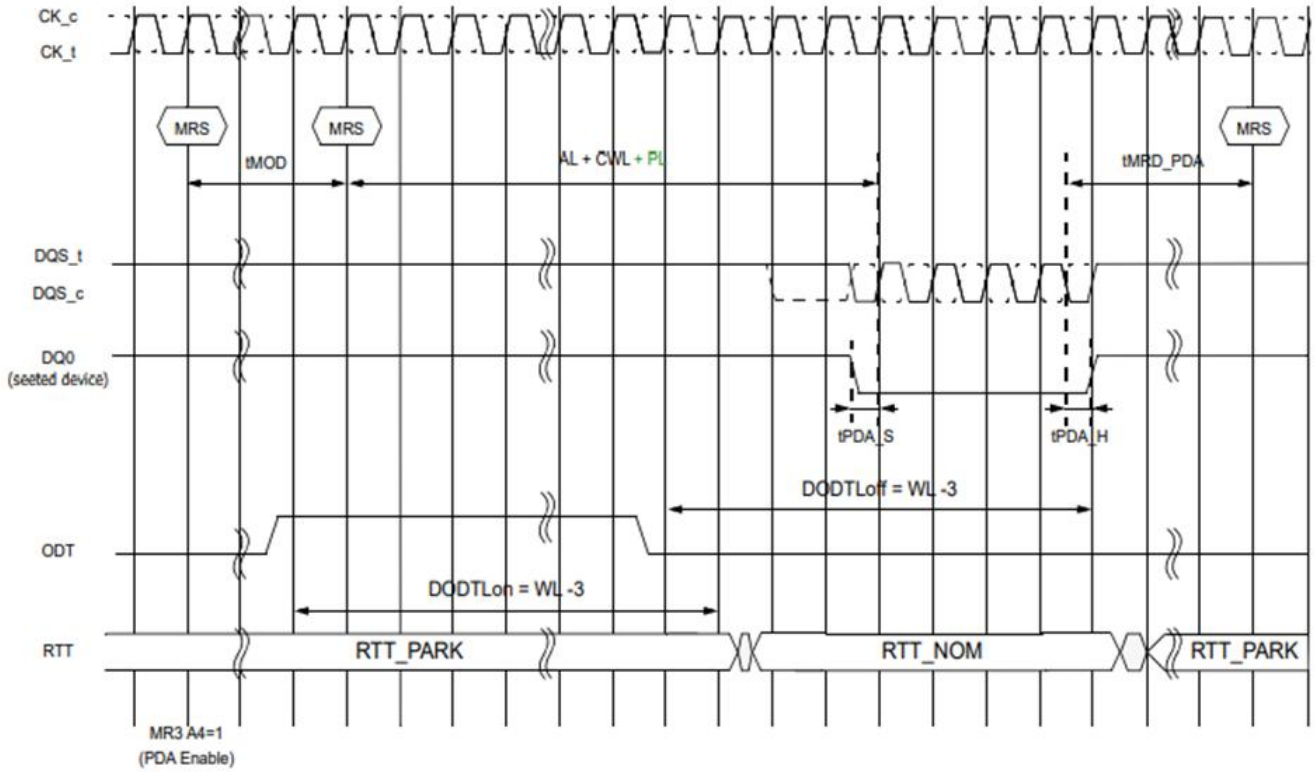
9. Remove the DRAM from Per DRAM Addressability mode by setting MR3 bit "A4=0" (this command requires DQ0=0 for x4/x8 configuration and DQ0L=0 for x16 configuration).

Note: Removing a DRAM from Per DRAM Addressability mode requires programming the entire MR3 when issuing the MRS command. This may affect the per-DRAM values programmed within a rank when the exit command is sent to that rank. To avoid this, the PDA enable/disable control bit is located in a mode register that has no per-DRAM addressability control. In Per DRAM Addressability mode, the DRAM captures DQ0 for x4 and x8, and DQ0 for x16, using DQS_t and DQS_c (for

x4 and x8), DQSL_c and DQSL_t (for x16), similar to a normal write operation. However, dynamic ODT is not supported. Therefore, special attention is needed for ODT settings. If RTT_NOM MR1 {A10:A9:A8} = Enable, then DDR4 SDRAM data termination must be controlled by the ODT pin, and the same timing parameters as defined in Table 20 for direct ODT functions apply. The VrefDQ value must be set to its midpoint or Vcent_DQ (midpoint) to properly capture DQ0 or DQ0L for entering PDA mode.

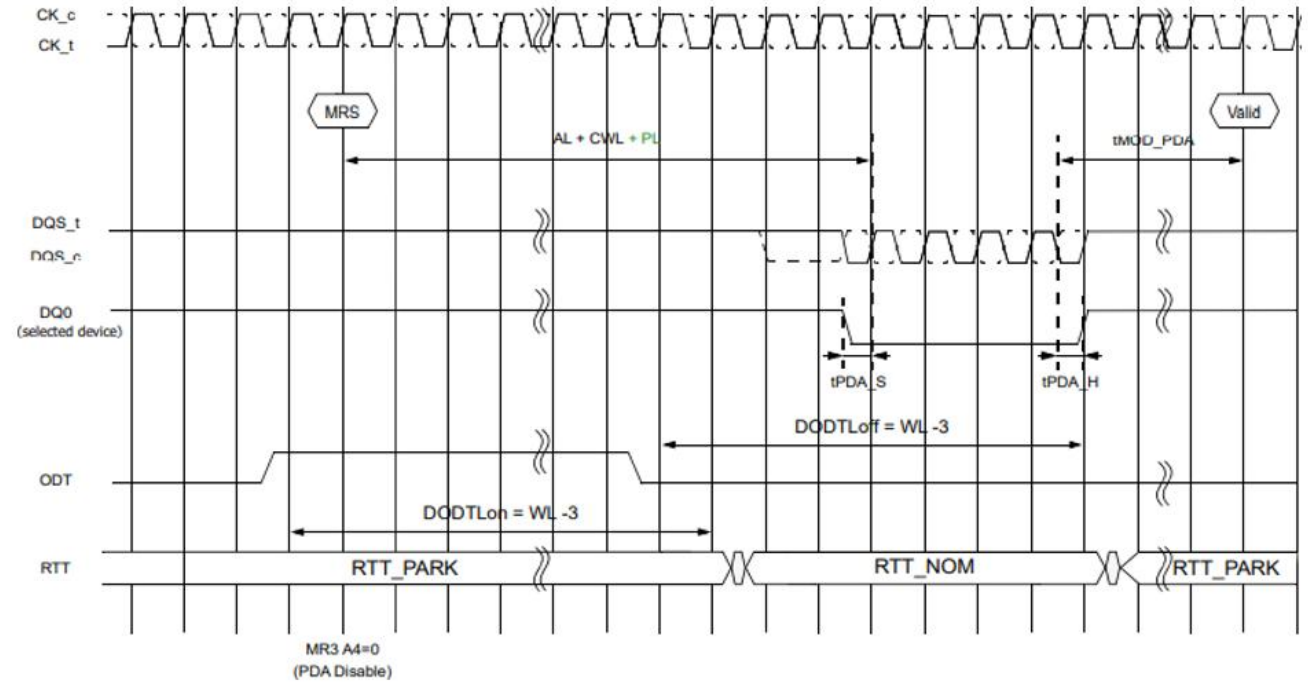
Table 20 ODT Timing Parameters Applied to PDA Mode

Symbol	Parameter
DODTLon	Direct ODT Turn-On Latency
DODTLoff	Direct ODT Turn-Off Latency
tADC	RTT Change Timing Jitter
tAONAS	Asynchronous RTT_NOM Turn-On Latency
tAOFAS	Asynchronous RTT_NOM Turn-Off Latency



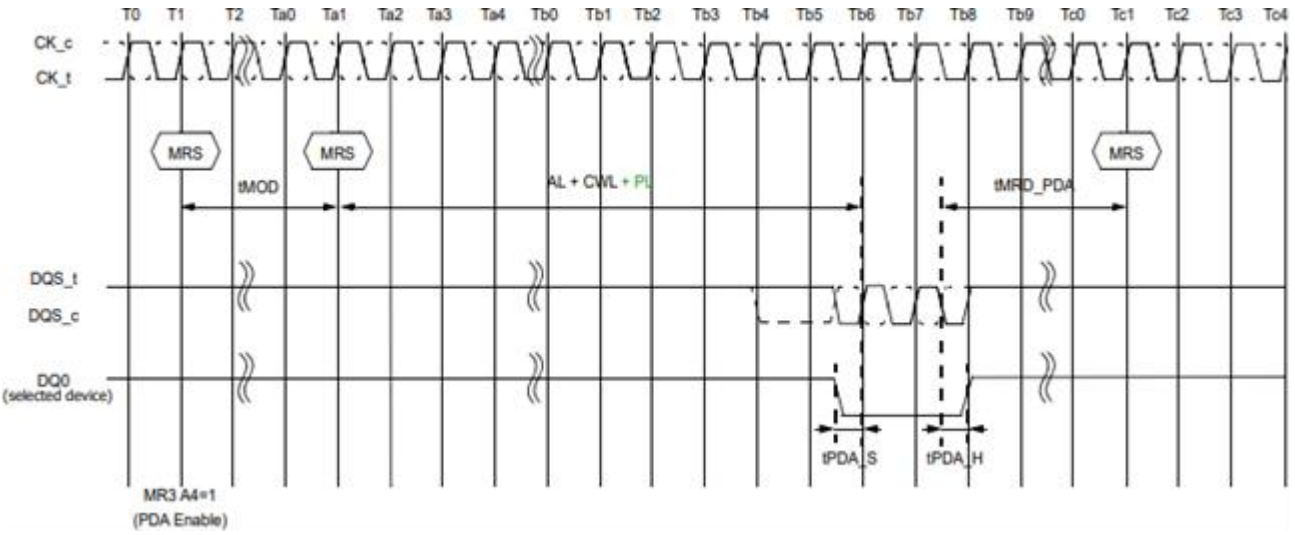
Note: RTT_PARK = Enabled, RTT_NOM = Enabled, Write Preamble Clock = 2tCK and DLL = On, with CA Parity enabled

Figure 2 Before MRS Per DRAM Addressability (PDA)



Note: RTT_PARK = Enabled, RTT_NOM = Enabled, Write Preamble Clock = 2tCK and DLL = On, with CA Parity enabled

Figure 3 MRS Per DRAM Addressability (PDA) Exit



Note: CA Parity enabled

Figure 4 PDA Using Burst Mutate 4

6.4 Write Leveling

For better signal integrity, DDR4 memory modules use a fly-by topology for command, address, control signals, and clock. The fly-by topology offers benefits in terms of reducing the number and length of stubs, but it also causes timing skew between the clock and strobe at each DRAM on the DIMM. This makes it difficult for the controller to maintain tDQSS, tDSS, and tDSH specifications. Therefore, DDR4 SDRAM supports the "write leveling" feature, allowing the controller to compensate for the skew. Under certain system conditions, if the host can maintain tDQSS, tDSS, and

tDSH specifications, this feature may not be needed.

The memory controller can use the "write leveling" feature and feedback from the DDR4 SDRAM to adjust the relationship between DQS_t – DQS_c and CK_t – CK_c. The memory controller participating in leveling must have adjustable delay on DQS_t – DQS_c to align the rising edge of DQS_t – DQS_c with the rising edge of the clock at the DRAM pins. The DRAM asynchronously feeds back CK_t – CK_c via the DQ bus, sampled by the rising edge of DQS_t – DQS_c. The controller repeatedly delays DQS_t – DQS_c until a 0-to-1 transition is detected. The DQS_t – DQS_c delay established through this exercise will ensure the tDQSS specification.

In addition to tDQSS, tDSS and tDSH specifications must be met. One approach to achieve this is to combine the actual tDQSS in the application with appropriate duty cycle and jitter on the DQS_t – DQS_c signal. Depending on the actual tDQSS in the application, the actual values of tDQSL and tDQSH may need to be better than the absolute limits provided in the "AC Timing Parameters" section to meet tDSS and tDSH specifications. The conceptual timing of this scheme is shown in Figure 5.

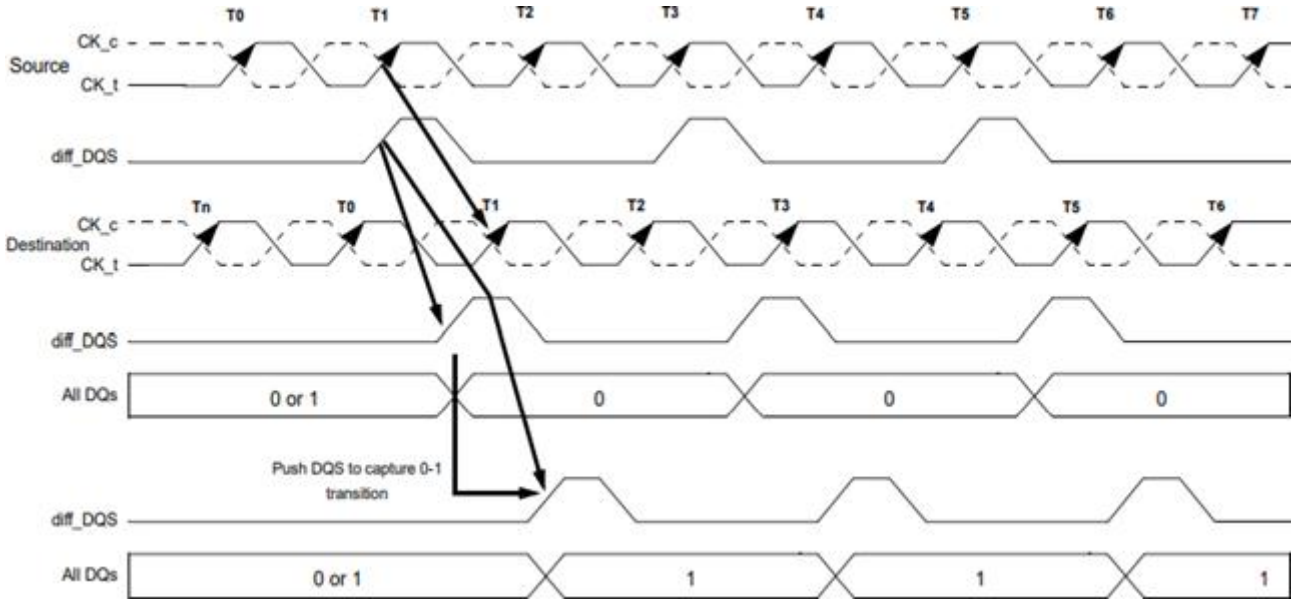


Figure 5 Write Leveling Concept

DQS_t – DQS_c is driven by the controller during leveling mode and must be terminated according to the rank populated in the DRAM. Similarly, the DQ bus driven by the DRAM must be terminated at the controller. All data bits should pass level feedback to the controller in DRAM configurations X4, X8, and X16. On X16 devices, the two byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be provided for each byte lane. The high data bits should provide feedback on the high diff_DQS (diff_UDQS) relationship, while the low data bits provide feedback on the low diff_DQS (diff_LDQS) relationship.

7. Absolute Maximum Ratings

7.1 Absolute Maximum DC Ratings

Table 21 DDR4 SDRAM Absolute Maximum DC Ratings

Symbol	Parameter	Range	Unit	Note
VDD	VDD voltage relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	VDDQ voltage relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	VPP voltage relative to Vss	-0.3 ~ 3.0	V	4
VIN, VOUT	Voltage on any pin relative to Vss (except VREFCA)	-0.3 ~ 1.5	V	1,3
TSTG	Temperature Range	-55 ~ +100	° C	1,2

Note:

1. Stresses greater than the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage temperature is the case surface temperature at the center/top of the DRAM. Measurement conditions refer to JESD51-2 standard.

3. VDD and VDDQ must always be within 300 mV of each other. VREFCA is not greater than 0.6 × VDDQ; when VDD and VDDQ are less than 500 mV, VREFCA may be equal to or less than 300 mV.

4. VPP must always be equal to or greater than VDD/VDDQ.

7.2 Operating Temperature Range

Table 22 Operating Temperature Range of DDR4 SDRAM Devices

Symbol	Parameter	Range	Unit	Note
TOPER	General Operating Temperature Range	0 to 85	° C	1,2
	Extended Temperature Range	85 to 95	° C	1,3
	Industrial Temperature Range	-40 to 95	° C	

Note:

1. Operating temperature TOPER is the case surface temperature at the center/top of the DRAM.

2. The "normal temperature range" specifies the temperature that supports all DRAM specifications. During operation, under all operating conditions, the DRAM case temperature must be maintained between 0° C and 85° C.

3. Some applications require the DRAM to operate in the extended temperature range of 85° C to 95° C. All specifications are guaranteed within this range, but the following additional conditions apply:

a. The refresh command frequency must be doubled, therefore reducing the refresh interval tREFI to 3.9 µs.

b. If self-refresh is required in the extended temperature range, the manual self-refresh mode with extended temperature range capability must be used (MR2 A6 = 0b, MR2 A7 = 1b).

8. DC Operating Conditions

Table 23 Recommended DC Operating Conditions

Symbol	Parameter	Range			Unit	Note
		Min.	Typ.	Max.		
VDD	Supply voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Output supply voltage	1.14	1.2	1.26	V	1,2,3
VPP		2.375	2.5	2.75	V	3

Note:

1. Under all conditions, VDDQ must be ≤ VDD.

2. VDDQ is synchronous with VDD. AC parameters are measured with VDD and VDDQ tied together.

3. DC bandwidth is limited to 20 MHz.

9. AC & DC Input Measurement Standards

9.1 AC and DC Logic Input Levels for Single-Ended Signals

Table 24: Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR4-2400		DDR4-2666/2933/3200		Unit
		Min.	Max.	Min.	Max.	
VIH.CA(DC75)	DC input logic high	VREFCA+75	VDD	VREF+65	VDD	mV
VIL.CA(DC75)	DC input logic low	VSS	VREFCA-75	VSS	VREF-65	mV
VIH.CA(AC100)	AC input logic high1	VREF+100	Note2	VREF+90	VDD	mV
VIL.CA(AC100)	AC input logic low1	Note2	VREF-100	VSS	VREF-90	mV
VREFCA(DC)	Reference Voltage for ADD, CMD inputs2,3	0.49*VDD	0.51*VDD	0.49*VDD	0.51*VDD	V

Note

1. See "Overshoot and Undershoot Specification" in 10.3

2. The AC peak noise on VREFCA must not allow VREFCA to deviate from VREFCA(DC) by more than ±1% VDD (approx. ± 12 mV reference)

3. Reference: approx. VDD/2 ±12 mV

9.2 AC & DC Input Measurement Standards: VREF Tolerance

The DC tolerance limits and AC noise limits for the reference voltage VREFCA are illustrated in Figure 6. It shows

a valid reference voltage VREF(t) as a function of time. (VREF denotes VREFCA.)

VREF(DC) is the linear average of VREF(t) over a very long time interval (e.g., 1 second). This average must meet the min/max requirements in Table 24. Additionally, VREF(t) may temporarily deviate from VREF(DC) by no more than ±1% VDD.

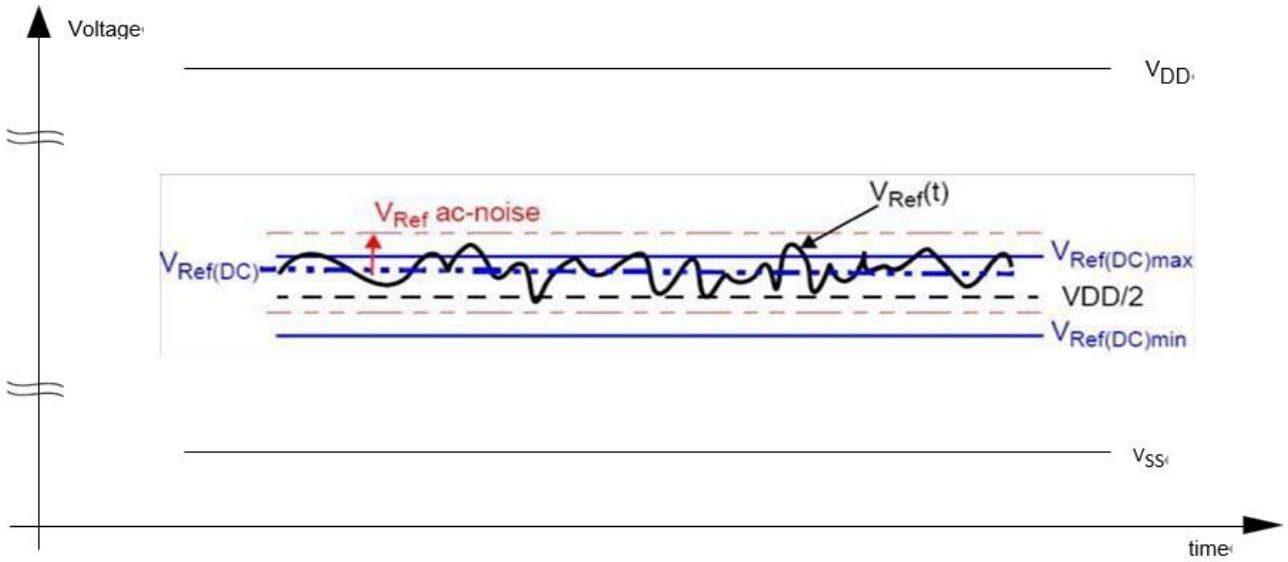


Figure 6 – Illustration of VREF(DC) Tolerance and VREF AC Noise Limits

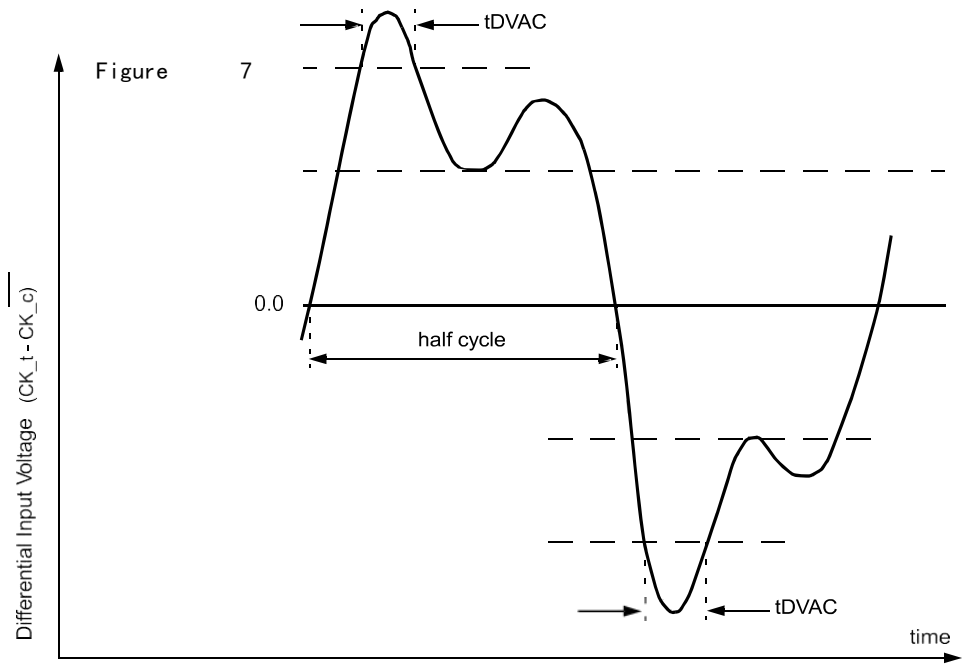
The voltage levels VIH(AC), VIH(DC), VIL(AC), and VIL(DC) for setup and hold time measurements depend on VREF. "VREF" should be understood as VREF(DC), as defined in Figure 6.

This indicates that DC variations of VREF affect the absolute voltage that a signal must reach to achieve a valid high or low level, thereby influencing the measurement of setup and hold times. The system timing and voltage budget need to account for the deviation of VREF(DC) from the optimal position within the data eye of the input signal.

This also explains that DRAM setup/hold specifications and derating values need to incorporate the time and voltage effects associated with VREF AC noise. The timing and voltage impacts resulting from AC noise on VREF up to the specified limit (+/-1% of VDD) are included in the DRAM timing and its associated derating.

9.3 AC & DC Logic Input Measurement Standards for Differential Signals

9.3.1 Differential Signal Definition



Note

1. Rising edge of differential signal from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic
2. Falling edge of differential signal from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic

9.3.2 Differential Swing Requirements for Clock (CK_t - CK_c)

Table 25 Differential AC & DC Input Standards

Symbol	Parameter	DDR4-2400, 2666, 2933, 3200		Unit	Note
		Min	Max		
VIHdiff	differential input high	0.120	Note 3	V	1
VILdiff	differential input low	Note 3	-0.120	V	1
VIHdiff(AC)	differential input high ac	2 x (VIH(AC) -VREF)	Note 3	V	2
VILdiff(AC)	differential input low ac	Note 3	2 x (VIL(AC) - VREF)	V	2

Note

1. Used to define the voltage slew rate of the differential signal.
2. For CK_t - CK_c, use VIHCA/VILCA(AC) of ADD/CMD and VREFCA.
3. These values are not defined; however, the differential signal CK_t - CK_c must be within the respective limits (VIHCA(DC) max, VILCA(DC) min of the single-ended signals) and the overshoot and undershoot limits.

Table 26: Allowable Ringback Time (tDVAC) for CK_t - CK_c

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(AC)| = 200mV		tDVAC [ps] @ |VIH/Ldiff(AC)| = TBDmV	
	Min	Max	Min	Max

> 4.0	120	-	TBD	-
4.0	115	-	TBD	-
3.0	110	-	TBD	-
2.0	105	-	TBD	-
1.8	100	-	TBD	-
1.6	95	-	TBD	-
1.4	90	-	TBD	-
1.2	85	-	TBD	-
1.0	80	-	TBD	-
< 1.0	80	-	TBD	-

9.3.3 Single-Ended Requirements for Differential Signals

Each individual component (CK_t, CK_c) of the differential signal must also meet certain single-ended signal requirements.

CK_t and CK_c must approximately reach VSEHmin / VSELmax (approximately equal to the AC levels {VIH.CA(AC) / VIL.CA(AC)} for ADD/CMD signals) in each half cycle.

Please note that the applicable AC levels for ADD/CMD may vary depending on speed grade, etc. For example, if the ADD/CMD signals use values different from VIH.CA(AC100)/VIL.CA(AC100), then these AC levels also apply to the single-ended signals CK_t and CK_c.

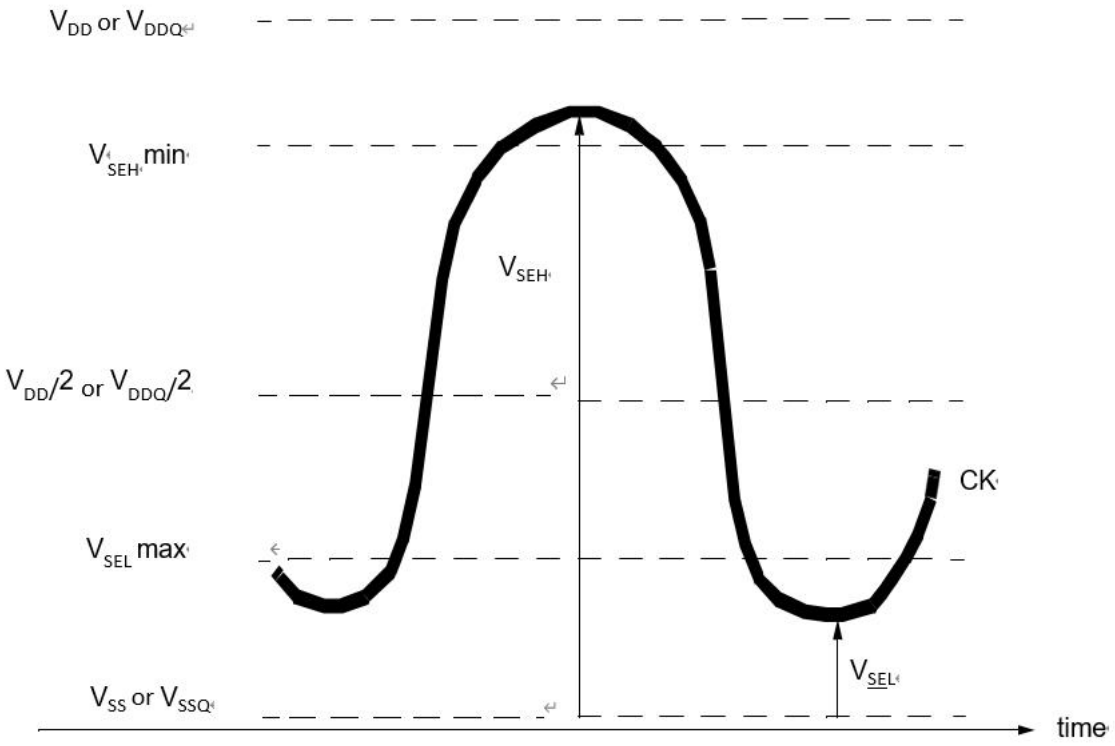


Figure 8 Single-Ended Requirements for Differential Signals

Note that the requirements for ADD/CMD signals relate to VrefCA, while the single-ended components of differential signals have requirements relative to VDD/2, nominally the same. The single-ended signals are used to measure setup time through transitions of AC levels. For the single-ended components of differential signals to meet the VSELmax requirement, VSEHmin is timing independent, but additional constraints are placed on the common-mode characteristics of these signals.onal constraints are placed on the common-mode characteristics of these signals.

Table 27 Single-Ended Levels for CK_t, CK_c

Symbol	Parameter	DDR4-2400/2666/2933/3200		Unit	Note
		Min	Max		
V_{SEH}	Single-ended high-level for CK_t , CK_c	(VDD/2)+90	Note 3	mV	1,2
V_{SEL}	Single-ended low-level for CK_t , CK_c	Note 3	(VDD/2)-90	mV	1,2

Note

1. For CK_t - CK_c, use ADD/CMD VIH.CA/VIL.CA(AC)
2. VIH(AC)/VIL(AC) for ADD/CMD are referenced to VREFCA
3. These values are not defined, but the single-ended signals CK_t and CK_c must be within their respective limits (VIH.CA(DC) max, VIL.CA(DC) min) and the overshoot and undershoot limits.

9.3.4 Address, Command, and Control Signal Overshoot and Undershoot Specifications

Table 28 Address, Command, and Control Signal AC Overshoot and Undershoot Specifications

Parameter	Symbol	Specification	Unit
		2400, 2666, 2933, 3200	
Maximum peak amplitude above VAOS	VAOSP	0.06	V
Overshoot area AAOS1 upper boundary	VAOS	VDD+0.24	V
Maximum peak amplitude allowed for undershoot	VAUS	0.30	V
Maximum overshoot area per 1 tCK above VAOS	AAOS2	0.0055	V/ns
Maximum overshoot area between VDD and VAOS per 1 tCK	AAOS1	0.1699	V/ns
Maximum undershoot area below VSS per 1 tCK	AAUS	0.1762	V/ns
(A0-A13, BG0-BG1, BA0-BA1, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT)			

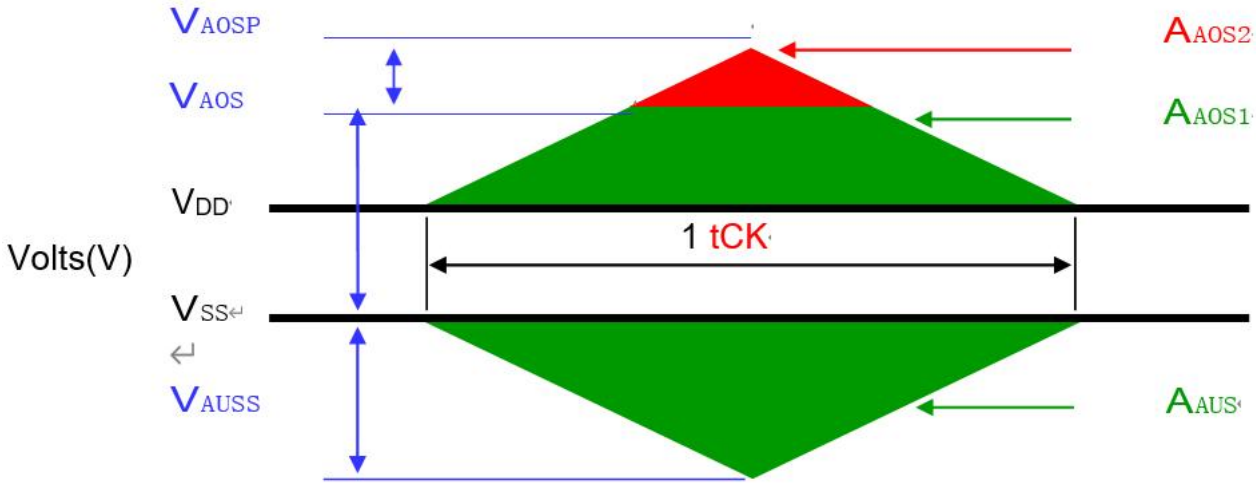


Figure 9: Overshoot and Undershoot Definition for Address, Command, and Control Signals

9.3.5 Clock Signal Overshoot and Undershoot Specifications

Table 29: Clock Signal AC Overshoot and Undershoot Specifications

Parameter	Symbol	Specification	Unit
		2400, 2666, 2933, 3200	
Maximum peak amplitude above VCOS	VCOSP	0.06	V
Upper Boundary of Overshoot Region ADOS1	VCOS	VDD+0.24	V
Maximum peak amplitude allowed for undershoot	VCUS	0.30	V
Maximum overshoot area above VCOS per UI	ACOS2	0.0025	V/ns
Maximum overshoot area between VDD and VDOS per UI	ACOS1	0.0750	V/ns
Maximum undershoot area below VSS per UI	ACUS	0.0762	V/ns
(CK_t, CK_c)			

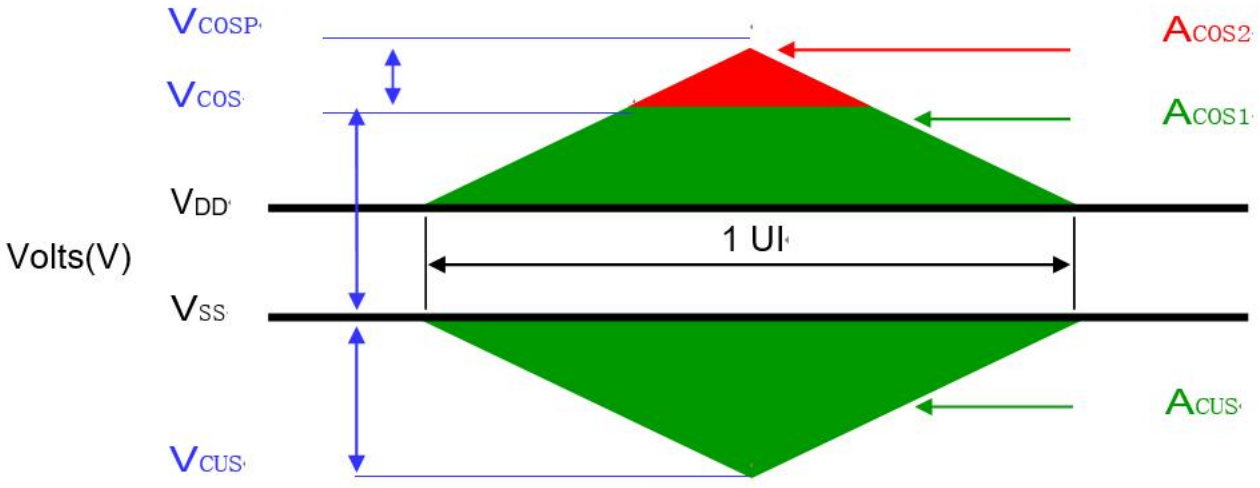


Figure 10: Overshoot and Undershoot Definition for Clock Signals

9.3.6 Overshoot and Undershoot Specifications for Data, Strobe, and Mask Signals

Table 30: AC Overshoot and Undershoot Specifications for Data, Strobe, and Mask Signals

Parameter	Symbol	Specification				Unit
		2400	2666	2933	3200	
Maximum Peak Amplitude Above VDOS	VDOSP	0.16				V
Upper Boundary of Overshoot Region ADOS1	VDOS	VDDQ+0.24				V
Undershoot Area ADUS1 Lower Boundary	VDUS	0.30				V
Maximum Peak Amplitude Below VDUS	VDUSP	0.10				V
Maximum Overshoot Area Above VDOS per 1 UI	ADOS2	0.0100	0.0129	0.0113	0.0100	V/ns
Maximum Undershoot Area per 1 UI Between VDDQ and VDOS	ADOS1	0.0700	0.0900	0.0788	0.0700	V/ns
Maximum Undershoot Area per 1 UI Between VSSQ and VDUS1	ADUS1	0.0700	0.0900	0.0788	0.0700	V/ns
Maximum Undershoot Area per 1 UI Below VDUS	ADUS2	0.0100	0.0129	0.0113	0.0100	V/ns
(DQ, DQS_t, DQS_c, DM_n, DBI_n, TDQS_t, TDQS_c)						

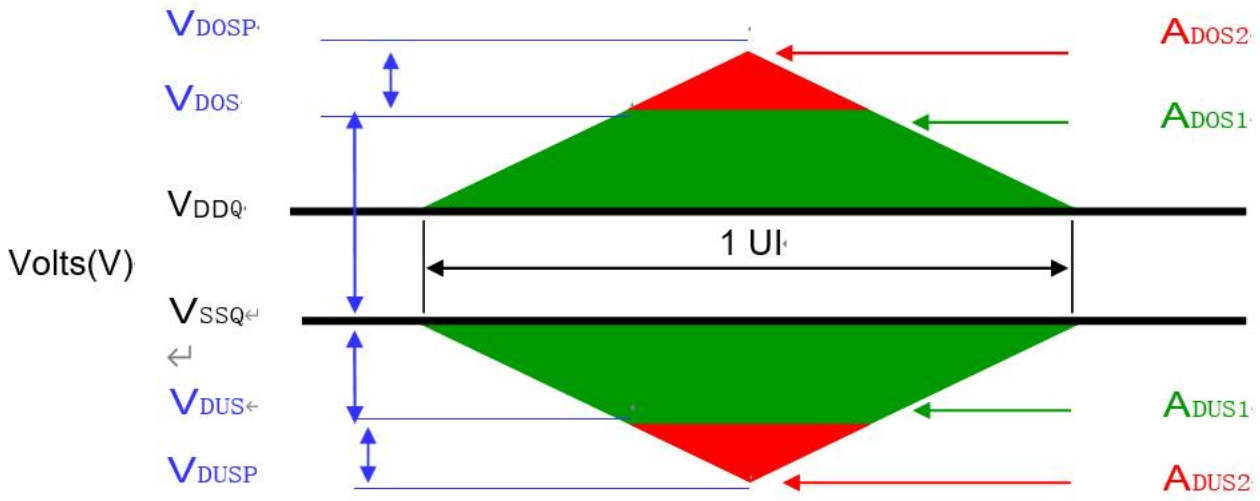


Figure 11 Overshoot and Undershoot Definition for Data, Strobe, and Mask Signals

9.4 Voltage Slew Rate

9.4.1 Voltage Slew Rate for Differential Input Signals (CK)

The definition and measurement of the input voltage slew rate for differential signals (CK_t, CK_c) are shown in Table 31 and Figure 12.

Table 31 Definition of Voltage Slew Rate for Differential Signals

Description	Measurement	Definition

	From	To	
Rising edge differential input slew rate (CK_t - CK_c)	VILdiffmax	VIHdiffmin	[VIHdiffmin - VILdiffmax] / DeltaTRdiff
Falling edge differential input slew rate (CK_t - CK_c)	VIHdiffmin	VILdiffmax	[VIHdiffmin - VILdiffmax] / DeltaTFdiff

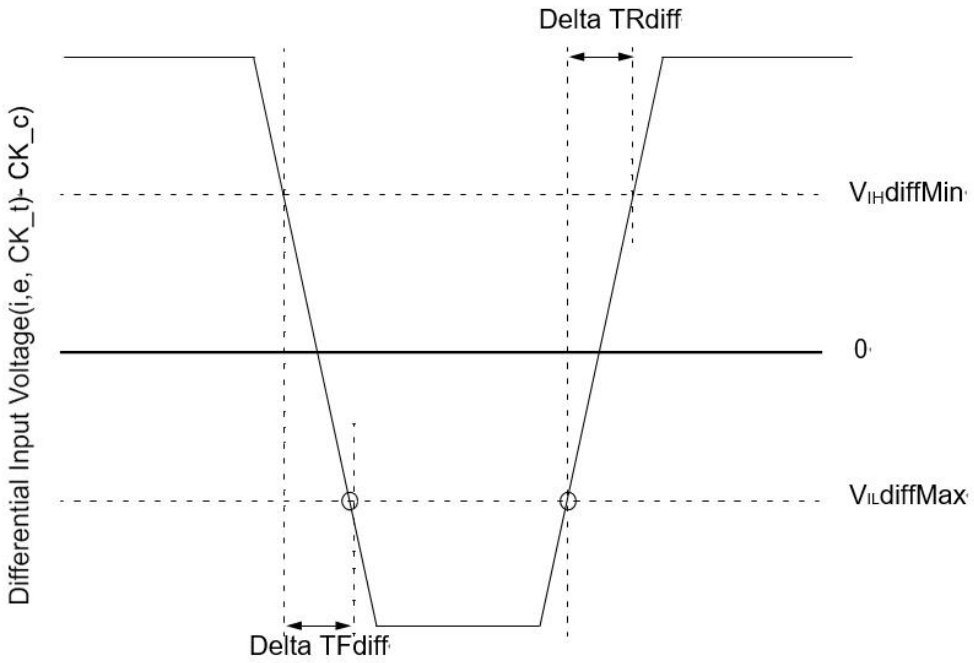


Figure 12 Differential Input Voltage Slew Rate Definition for CK_t and CK_c

9.4.2 Slew Rate for Single-Ended Input Signals (CMD/ADD)

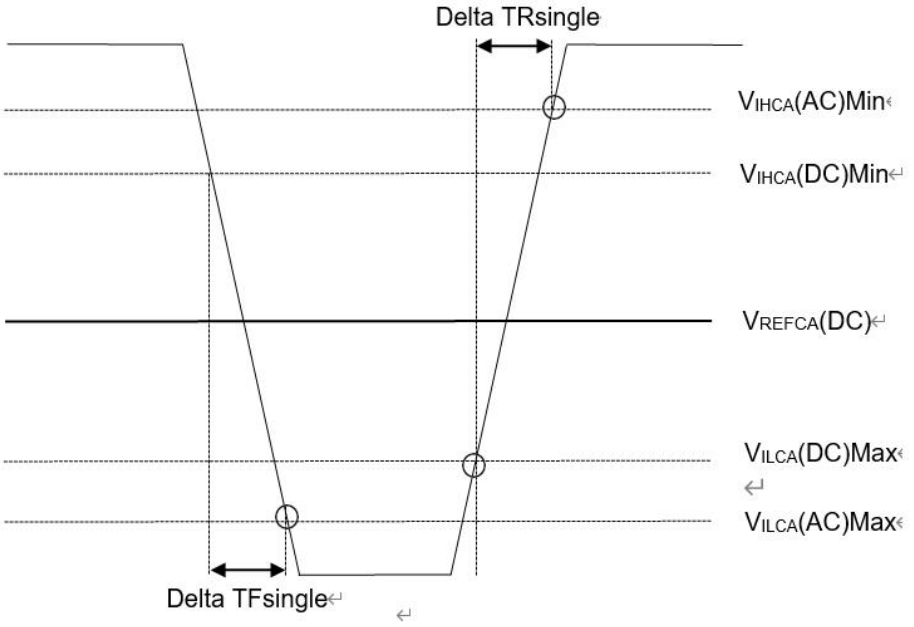


Figure 13 Slew Rate Definition for Single-Ended Input Signals (CMD/ADD)

Note

1. Rising edge single-ended input slew rate = {VIHCA(AC)Min - VILCA(DC)Max} / Delta TRsingle-ended.
2. Falling edge single-ended input slew rate = {VIHCA(DC)Min - VILCA(AC)Max} / Delta TFsingle-ended.
3. The rising edge of a single-ended signal from VILCA(DC)Max to VIHCA(DC)Min must be monotonic.
4. The falling edge of a single-ended signal from VIHCA(DC)Min to VILCA(DC)Max must be monotonic.

9.5 Differential Input Cross Point Voltage

To ensure tight setup and hold times and output skew parameters relative to clock, the cross point voltage of each differential input signal (CK_t, CK_c) must meet the requirements in Table 32. Differential input cross point voltage VIX is measured from the actual cross point of the true and complementary signals to the midpoint between VDD and VSS.

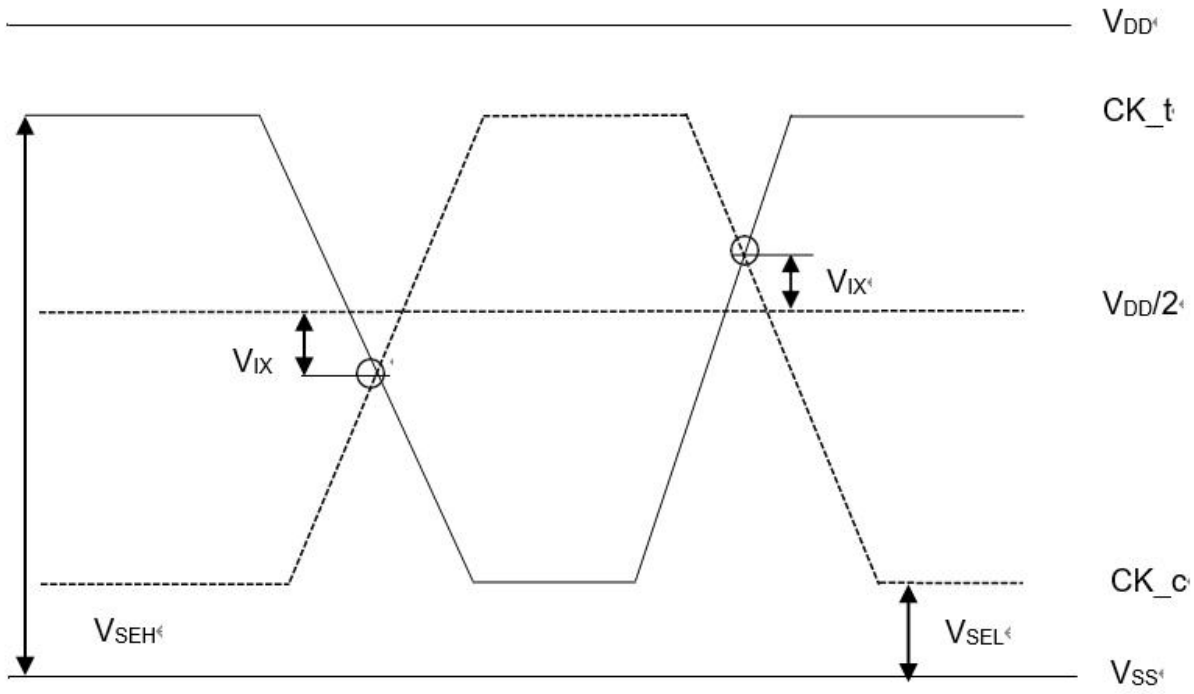


Figure 13 VIX Definition (CK)

Table 32 Cross Point Voltage for Differential Input Signals (CK)

Parameter	Symbol	Input Level	DDR4-2400, 2666, 2933, 3200	
			Min	Max
For CK_t, CK_c Differential Input Cross Point Voltage Relative to	VIX(CK)	VSEH>VDD/2+135mV	-	110mV
		VDD/2+90mV≦VSEH≦VDD/2+135mV	-	(VSEH-VDD/2)-30mV

VDD/2		VDD/2-135mV≦VSEL≦VDD/2-90mV	-(VDD/2-VSEL)+30mV	-
		VSEL≦VDD/2-135mV	-110mV	-

9.6 CMOS Rail-to-Rail Input Levels

9.6.1 RESET_n Signal CMOS Rail-to-Rail Input Levels

Table 33: RESET_n Signal CMOS Rail-to-Rail Input Levels

Parameter	Symbol	Min	Max	Unit	Notes
AC Input High Voltage	VIH(AC)_RESET	0.8*VDD	VDD	V	6
DC Input High Voltage	VIH(DC)_RESET	0.7*VDD	VDD	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDD	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDD	V	7
Rise Time	TR_RESET	-	1	us	4
Reset Pulse Width	tPW_RESET	1.0	-	us	3,5

Note

1. Once RESET_n is registered low, during tPW_RESET, the RESET_n level must be kept below VIL(DC)_RESET; otherwise, the SDRAM may not reset.
2. Once RESET_n is registered high, the RESET_n level must be kept above VIH(DC)_RESET; otherwise, SDRAM operation cannot be guaranteed until RESET_n is asserted low during reset.
3. RESET is destructive to data contents.
4. During the low-to-high level transition, ramp reversal (ringing) is not allowed.
5. This definition applies only to the "Reset procedure after power stabilization".
6. Overshoot may occur. It should be limited by the absolute maximum DC rating.
7. Undershoot may occur. It should be limited by the absolute maximum DC rating.

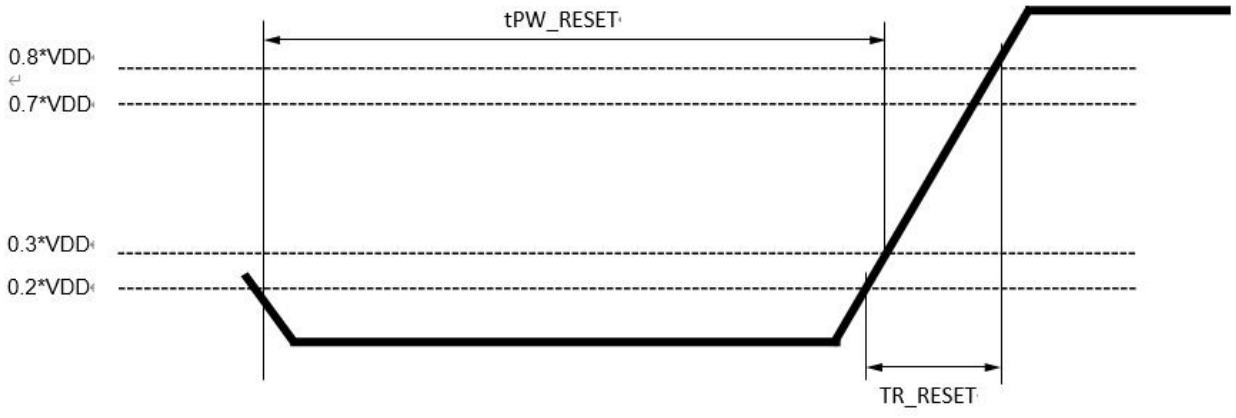


Figure 14 Definition of RESET_n Input Level Slew Rate

9.7 Differential AC and DC Logic Input Levels for DQS

9.7.1 Differential Signal Definition

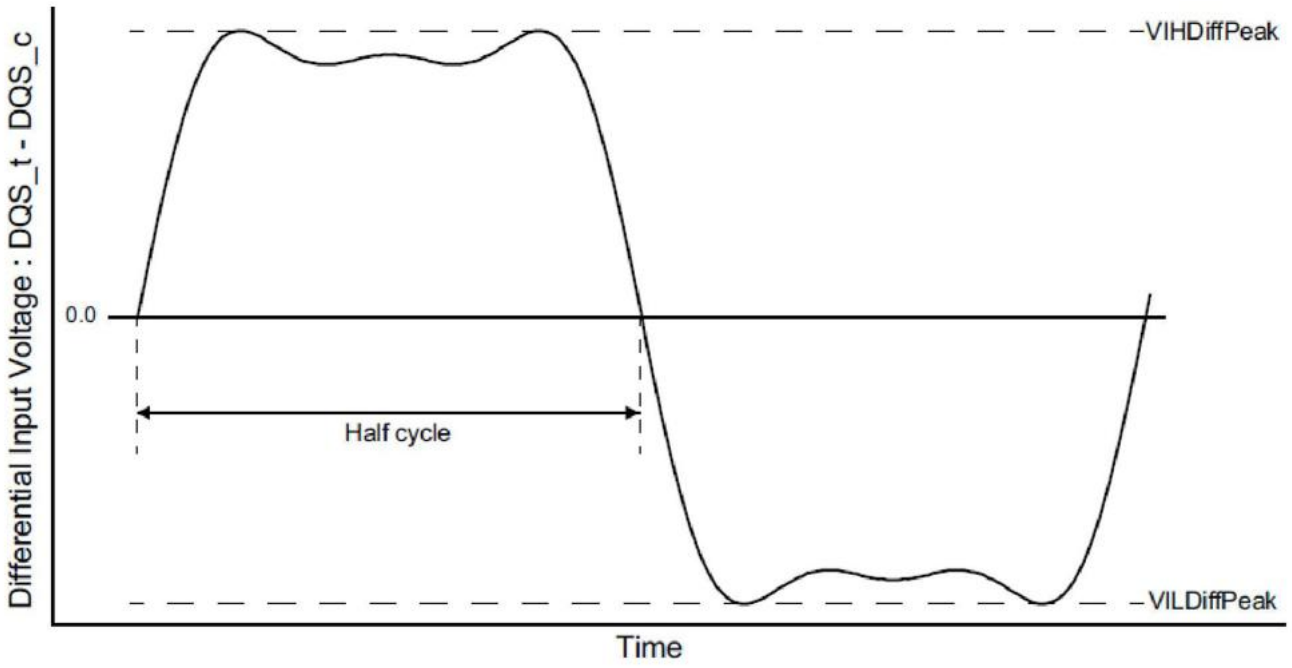


Figure 15 Definition of Differential DQS AC Swing Levels

9.7.2 Differential Swing Requirements for DQS (DQS_t - DQS_c)

Table 34 Differential AC and DC Input Levels for DQS

Symbol	Parameter	2400		2666		2933		3200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
VIHDiffPeak	VIH.DIFF.Peak Voltage	160	Note 2	150	VDDQ	145	VDDQ	140	VDDQ	mV	1
VILDiffPeak	VIL.DIFF.Peak Voltage	Note 2	-160	VSSQ	-150	VSSQ	-145	VSSQ	-140	mV	1

Note:

1. Used to define the slew rate of the differential signal.
2. These values are not defined; however, the differential signals DQS_t - DQS_c need to be within the respective limits of the overshoot and undershoot specifications for single-ended signals.

9.7.3 Peak Voltage Calculation Method

The peak voltage of the differential DQS signal is calculated using the following formula.

VIH.DIFF.Peak Voltage = Max(f(t))

VIL.DIFF.Peak Voltage = Min(f(t))

f(t) = VDQS_t - VDQS_c

The positive peak voltage (VIH.DIFF) is defined as Max(f(t)) and the negative peak voltage (VIL.DIFF) is defined as Min(f(t)) across all UIs. These values are used to determine the midpoint of the ±35% window of the non-monotonic signal reference.

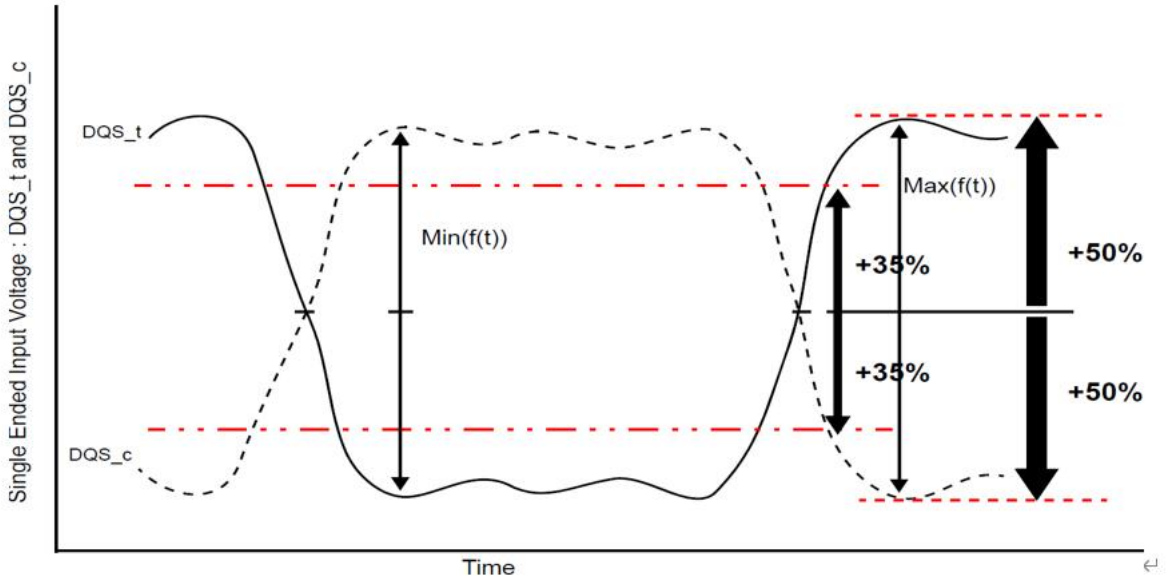


Figure 16: Definition of Differential DQS Peak Voltage and Non-Monotonic Signal Range

9.7.4 Differential Signal Input Crosspoint Voltage

To meet the strict RxMask input requirements and the output skew parameters relative to the data strobe, the crosspoint voltage of the differential input signals (DQS_t, DQS_c) must satisfy the requirements in Table 35. The differential input crosspoint voltage VIX_DQS (VIX_DQS_FR and VIX_DQS_RF) is measured from the actual crosspoint of DQS_t and DQS_c relative to VDQSmid of the DQS_t and DQS_c signals.

VDQSmid is the midpoint of the minimum levels reached by the DQS_t and DQS_c signals after transition, denoted by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid and the highest horizontal tangent below VDQSmid of the transitioning DQS signal.

Edges of non-monotonic transition signals may be exempted or not used for determining the horizontal tangent, provided that the edge occurs within ±35% of the midpoint of the VIH.DIFF peak voltage (DQS_t rising) or VIL.DIFF peak voltage (DQS_c rising), see Figure 16. Secondary horizontal tangents resulting from ringback transitions are also exempted when determining the horizontal tangent. That is, for a falling transition segment, the horizontal tangent is determined from its negative-slope to zero-slope transition segment (point a in Figure 17); the horizontal tangent derived from the ringback's positive-slope to zero-slope transition segment (point B in Figure 17) is not a valid horizontal tangent. For a rising transition segment, the horizontal tangent from the positive-slope to zero-slope transition segment (point C in Figure 17) is valid; the horizontal tangent from the ringback's negative-slope to zero-slope transition segment

(point D in Figure 17) is not a valid horizontal tangent.

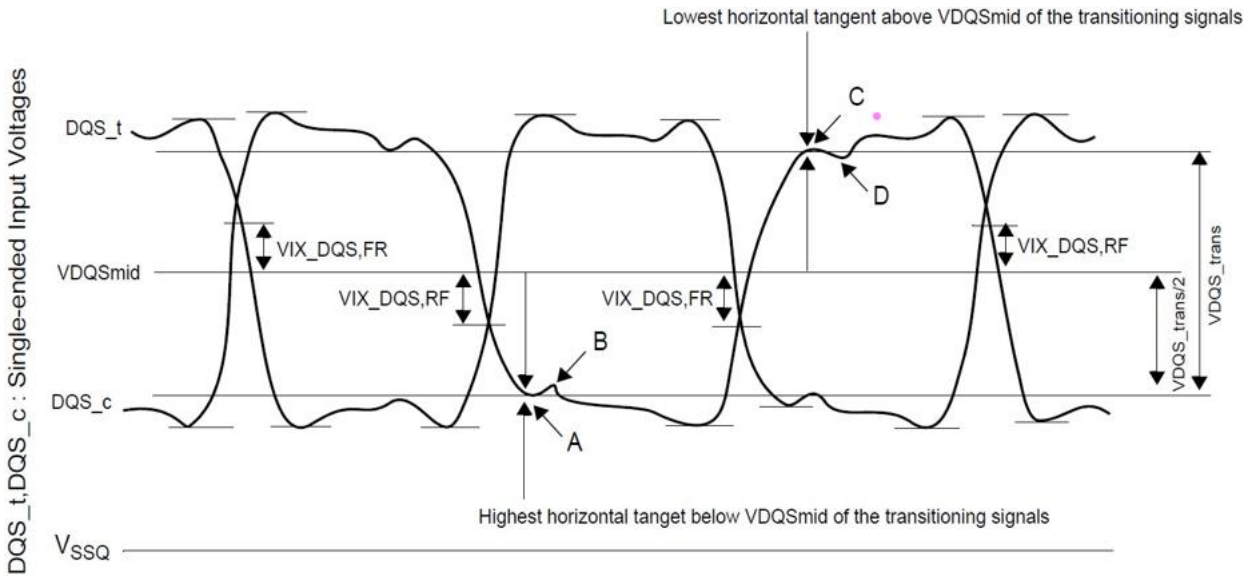


Figure 17 Vix Definition (DQS)

Figure 35 DQS Differential Input Signal Crosspoint Voltage

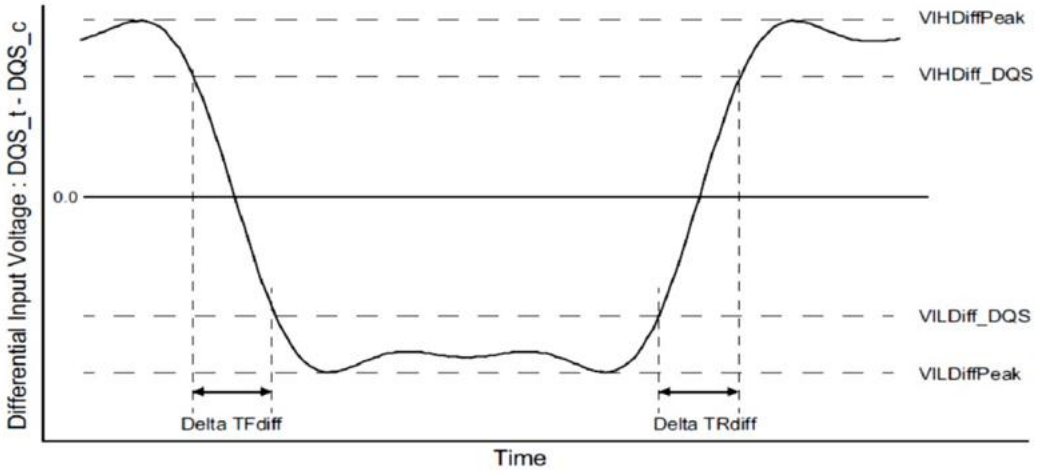
Symbol	Parameter	2400, 2666, 2933, 3200		Unit	Notes
		Min	Max		
Vix_DQS_ratio	DQS_t and DQS_c intersect at the midpoint of the DQS_t and DQS_c signal swings.	-	25	%	1, 2
VDQSmid_to_Vcent	Offset of VDQSmid relative to Vcent_DQ (midpoint)	-	Min(VIHdiff, 50)	mV	3, 4, 5

Note

1. Vix_DQS_Ratio is the DQS VIX crossover (Vix_DQS_FR or Vix_DQS_RF) divided by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid and the highest horizontal tangent below VDQSmid of the transitioning DQS signal.
2. If DQS_t and DQS_c are matched in drive and path, VDQSmid will be similar to the VREFDQ internal setting value obtained during VREF training.
3. The maximum limit must not exceed the smaller of the VIHdiff maximum limit or 50 mV.
4. When switching data, the VIX measurement applies only to transitions of the DQS_t and DQS_c signals; preamble and high-impedance states are not applicable.
5. The parameter VDQSmid is defined for simulation and ATE test purposes and is not expected to be tested in the system.

9.7.5 Differential Input Voltage Slew Rate

The definition and measurement of the input voltage slew rate for differential signals (DQS_t, DQS_c) are shown in Figure 17 and Figure 18.



Note:

1. The rising edge of the differential signal from VILDiff_DQS to VIHDiff_DQS must have a monotonic slope.
2. The falling edge of the differential signal from VIHDiff_DQS to VILDiff_DQS must have a monotonic slope.

Figure 18 Definition of Differential Input Voltage Slew Rate for DQS_t and DQS_c

Table 36 Definition of Differential Input Voltage Slew Rate for DQS_t and DQS_c

Description	Test		Definition
	From	To	
Rising edge differential input voltage slew rate (DQS_t - DQS_c)	VILDiff_DQS	VIHDiff_DQS	|VILDiff_DQS - VIHDiff_DQS|/DeltaTRdiff
Falling edge differential input voltage slew rate (DQS_t - DQS_c)	VIHDiff_DQS	VILDiff_DQS	|VILDiff_DQS - VIHDiff_DQS|/DeltaTFdiff

Table 37: Differential Input Levels for DQS_t and DQS_c

Symbol	Parameter	2400		2666		2933		3200		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
VIHDiff_DQS	Differential Input High	130	-	120	-	115	-	110	-	mV
VILDiff_DQS	Differential Input Low	-	-130	-	-120	-	-115	-	-110	mV

Table 38: Differential Input Voltage Slew Rate for DQS_t and DQS_c

Symbol	Parameter	2400/2666/2933/3200	Unit

		Min	Max	
SRIdiff	Differential Input Slew Rate	3	18	V/ns

10. AC & DC Output Measurement Standards

10.1 Output Driver DC Electrical Characteristics

The DDR4 driver supports two different Ron values. These Ron values are referred to as strong (low Ron) and weak mode (high Ron). The functional representation of the output buffer is shown in the figure below. The output buffer impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RONPu and RONPd) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|Iout|}$$ Calculated with RONPd off

$$RON_{Pd} = \frac{Vout}{|Iout|}$$ Calculated with RONPu off

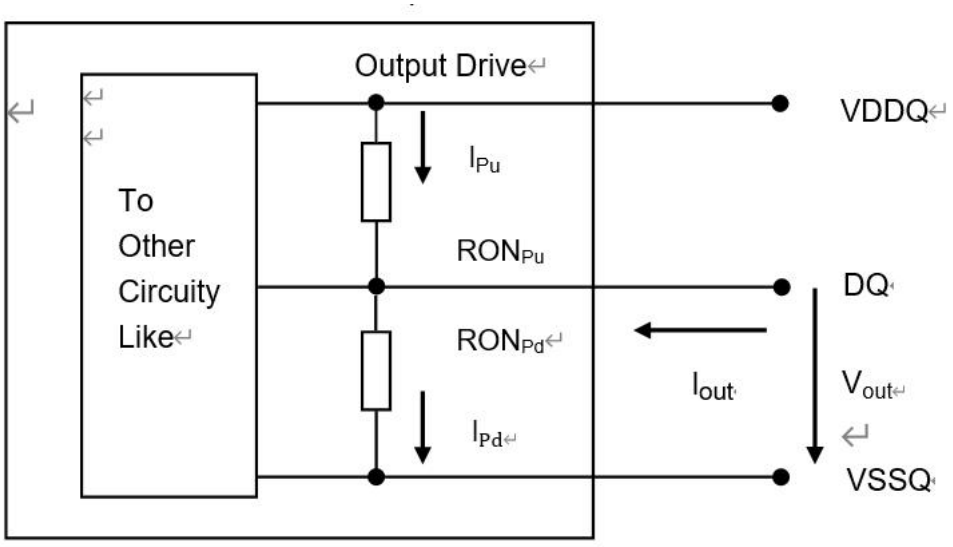


Figure 39 Output Driver

Table 42 Output Driver DC Electrical Characteristics, assuming RZQ=240 ohm; full operating temperature range; proper ZQ calibration completed.

	Resistance Value	Output Voltage	Min	Nom	Max	Unit	Notes
	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.9	1	1.25	RZQ/7	1,2

34Ω	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.9	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5*VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2
Pull-up and Pull-down Mismatch, MMPuPd		VOMdc= 0.8* VDDQ	-10	-	10	%	1,2,3,4
DQ-DQ Byte Variation Pull-up Mismatch, MMPudd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4
DQ-DQ Byte Variation Pull-down Mismatch, MMPddd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4

Note:

Tolerance limits are specified after calibration at stable voltage and temperature. If temperature or voltage changes after calibration, the behavior of the tolerance limits is described in the Voltage and Temperature Sensitivity sections below (TBD).

Pull-up and pull-down output driver impedance is recommended to be calibrated to 0.8 * VDDQ. Other calibration schemes can be used to meet the linearity specifications above, e.g., at 0.5 * VDDQ and 1.1 * VDDQ.

Pull-up Pull-down Mismatch Measurement Definition: Measure RONPu and RONPD at 0.8 * VDDQ respectively; RONnom is the nominal RON value.

Ratio of RON variation range to RON nominal value within a given device, including DQS_t and DQS_c.

For x16 devices, this parameter applies to upper byte and lower byte.

10.1.1 Alert_n Output Driver Characteristics

The functional representation of the buffer is shown in the figure below. The output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|Iout|}$$ Calculated with RONpu off

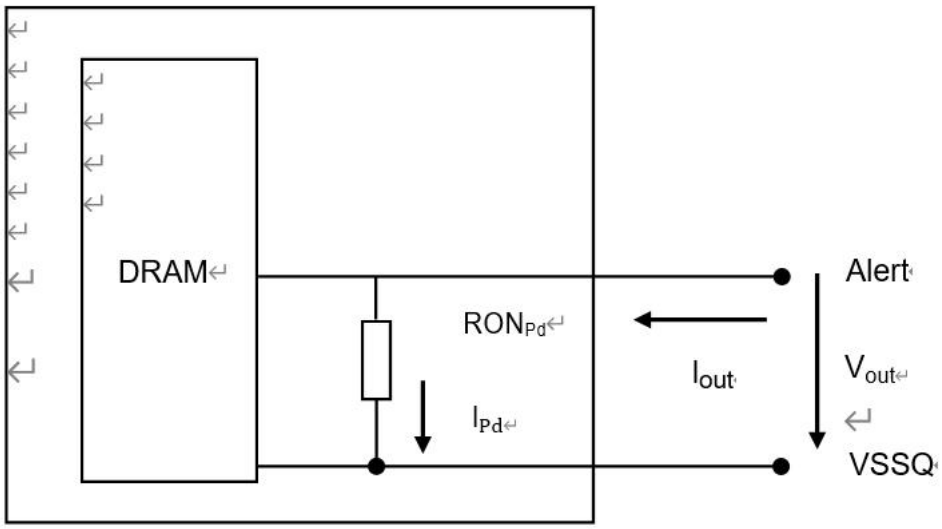


Figure 19 Alert_n Output Driver

Table 40 Alert_n Output Driver DC Electrical Characteristics

Resistance	Output Voltage	Min	Max	Unit	Notes
RON	VOLdc= 0.1* VDDQ	0.3	1.2	34Ω	1
	VOMdc= 0.8* VDDQ	0.4	1.2	34Ω	1
	VOHdc= 1.1* VDDQ	0.4	1.4	34Ω	1
Note: VDDQ voltage refers to VDDQ DC specification. VDDQ DC definition is pending.					

10.1.2 Connectivity Test (CT) Mode Output Driver Characteristics

In Connectivity Test (CT) mode, the following output driver impedance RON will be applied to the test output pins.

The single pull-up and pull-down resistances (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu_CT} = \frac{VDDQ - Vout}{|Iout|}$$

$$RON_{Pd_CT} = \frac{Vout}{|Iout|}$$

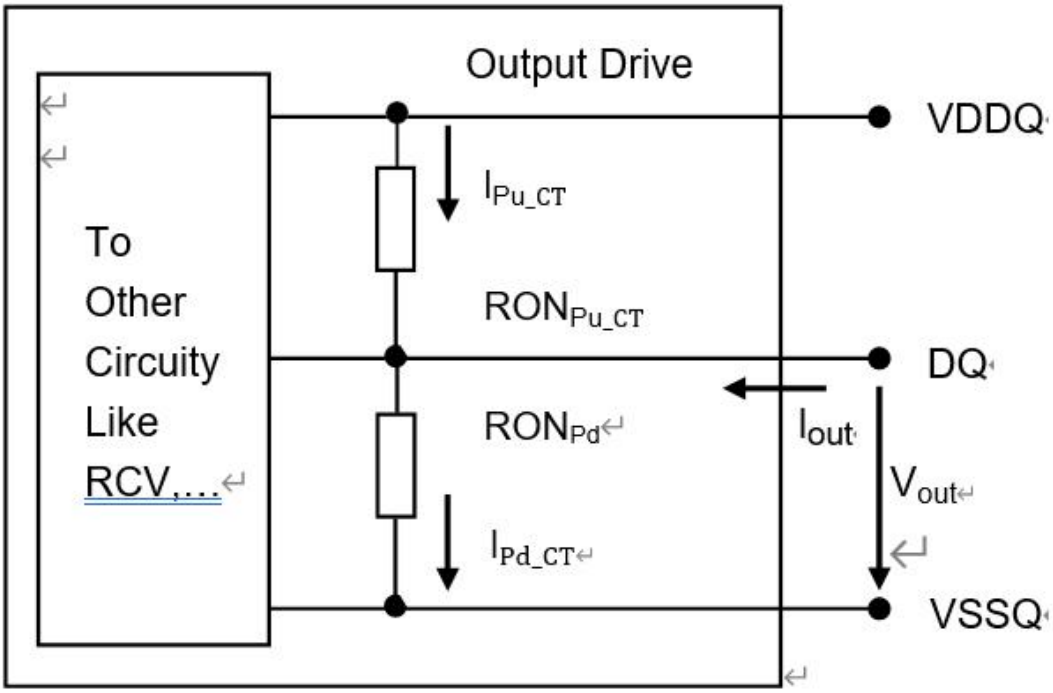


Figure 42 Connectivity Test (CT) Output Driver

Table 41 Connectivity Test (CT) Output Driver DC Electrical Characteristics

	Resistance	Output Voltage	Max	Unit	Unit
34Ω	RONPd_CT	VOBdc = 0.2 x VDDQ	1.9	34Ω	1
		VOLdc = 0.5 x VDDQ	2.0	34Ω	1
		VOMdc = 0.8 x VDDQ	2.2	34Ω	1
		VOHdc = 1.1 x VDDQ	2.5	34Ω	1
	RONPu_CT	VOBdc = 0.2 x VDDQ	2.5	34Ω	1
		VOLdc = 0.5 x VDDQ	2.2	34Ω	1
		VOMdc = 0.8 x VDDQ	2.0	34Ω	1
		VOHdc = 1.1 x VDDQ	1.9	34Ω	1
connectivity test mode					

10.2 Single-Ended AC and DC Output Levels

Table 42 Single-Ended AC and DC Output Levels

Symbol	Parameter	2400/2666/2933/3200	Unit	Notes
VOH (DC)	DC Output High Measurement Level (IV curve linearity)	1.1 x VDDQ	V	
VOM(DC)	DC Output Mid Measurement Level (IV curve linearity)	0.8 x VDDQ	V	

VOL(DC)	DC Output Low Measurement Level (from IV curve linearity)	0.5 x VDDQ	V	
VOH (AC)	AC output high measurement level (for output slew rate)	(0.7 + 0.15) x VDDQ	V	1
VOL (AC)	AC output low measurement level (for output slew rate)	(0.7 - 0.15) x VDDQ	V	1

Note: The ±0.15×VDDQ swing is based on approximately 50% of the static single-ended output peak-to-peak swing, with driver impedance of RZQ/7Ω and effective test load of 50Ω to VTT = VDDQ.

10.3 Differential AC and DC Output Levels

Table 43 Differential AC and DC Output Levels

Symbol	Parameter	2400/2666/2933/3200	Unit	Notes
VOHdiff(AC)	AC differential output high measurement level (for output slew rate)	+0.3 x VDDQ	V	1
VOLdiff(AC)	AC differential output low measurement level (for output slew rate)	-0.3 x VDDQ	V	1

Note: The ±0.3×VDDQ swing is based on approximately 50% of the static differential output peak-to-peak swing, with driver impedance of RZQ/7Ω and effective test load of 50Ω to VTT = VDDQ at each differential output.

10.4 Single-Ended Output Voltage Slew Rate

Under the reference load for timing measurements, the output voltage slew rate for the falling edge and rising edge of single-ended signals between VOL(AC) and VOH(AC) is defined and measured, as shown in Table 44 and Figure 20.

Table 44: Single-Ended Output Voltage Slew Rate Definition

Description	Measurement		Definition
	From	To	
Single-ended output voltage slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC)-VOL(AC)] / Delta Trse
Single-ended output voltage slew rate for falling edge	VOH(AC)	VOL(AC)	[VOH(AC)-VOL(AC)] / Delta Tfse

Note: The output voltage slew rate is guaranteed by design and characterization and may not be subject to production test.

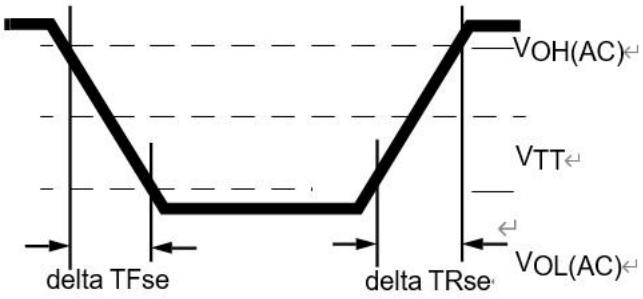


Figure 20: Single-Ended Output Voltage Slew Rate Definition

Table 45: Single-Ended Output Voltage Slew Rate

Parameter	Symbol	2400/2666/2933/3200		Unit
		Min	Max	
Single-ended Output Slew Rate	SRQse	4	9	V/ns

SR: Slew Rate

Q: Output Data (e.g., DQ, indicating data input/output)

se: Single-ended Signal

For Ron = RZQ/7 setting

Note

1. In both cases, the maximum slew rate of 12 V/ns applies to a single DQ signal within a byte lane.

- Case 1 is defined for a single DQ signal within a byte lane that is switching in one direction (high-to-low or low-to-high), while all remaining DQ signals in the same byte lane are static (i.e., they remain high or low).

- Case 2 is defined as a single DQ signal within a byte lane switching in one direction (high-to-low or low-to-high), while all remaining DQ signals in the same byte lane switch in the opposite direction (i.e., low-to-high or high-to-low, respectively). For the remaining DQ signals switching in the opposite direction, the standard maximum limit of 9 V/ns applies.

10.5 Differential Output Slew Rate

Under the reference load for timing measurements, the output slew rate of the differential signal on the falling edge and rising edge between VOLdiff(AC) and VOHdiff(AC) is defined and measured, as shown in Table 46 and Figure 21.

Table 46: Differential Output Voltage Slew Rate Definition

Description	Measurement		Definition
	From	To	
Differential Output Voltage Slew Rate for Rising Edge	VOLdiff(AC)	VOHdiff(AC)	[VOHdiff(AC)-VOLdiff(AC)] / Delta Trdiff

Differential Output Voltage Slew Rate for Falling Edge	VOHdiff(AC)	VOLdiff(AC)	[VOHdiff(AC)-VOLdiff(AC)] /Delta Tfdiff

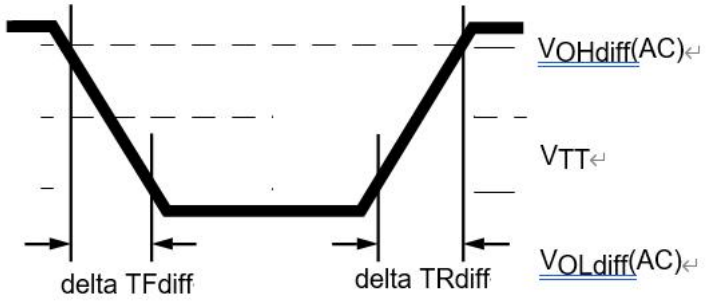


Figure 21: Differential Output Voltage Slew Rate Definition

Table 47: Differential Output Voltage Slew Rate

Parameter	Symbol	2400/2666/2933/3200		Unit
		Min	Max	
Differential output voltage slew rate	SRQdiff	8	18	V/ns

SR: Voltage slew rate

Q: Query output (e.g., DQ represents data input, query output)

diff: Differential signal

For Ron = RZQ/7 setting

10.6 Single-ended AC and DC Output Levels for Connectivity Test Mode

In connectivity test mode, the DDR4 SDRAM output signals shall apply the following output parameters.

Table 48 Single-ended AC and DC Output Levels for Connectivity Test Mode

Symbol	Parameter	2400/2666/2933/3200	Unit	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOB(DC)	DC output below measurement level (for IV curve linearity)	0.2 x VDDQ	V	

VOH(AC)	AC output high measurement level (for output slew rate)	VTT + (0.1 x VDDQ)	V	1
VOL(AC)	AC output low measurement level (for output slew rate)	VTT - (0.1 x VDDQ)	V	1

Note

1. Effective test load 50Ω terminated to VTT = 0.5*VDDQ.

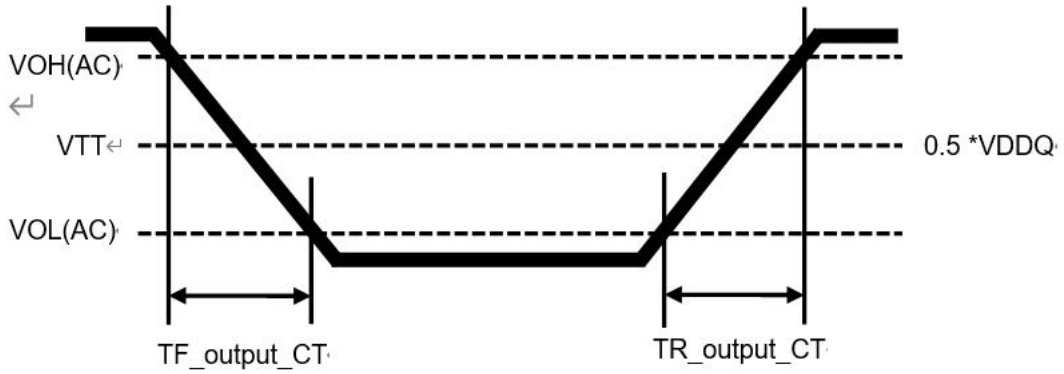


Figure 22 Output Voltage Slew Rate Definition for Connectivity Test Mode

Table 49 Single-Ended Output Slew Rate for Connectivity Test Mode

Parameter	Symbol	2400/2666/2933/3200		Unit	Notes
		Min	Max		
Output signal fall time	TF_output_CT	-	10	ns/V	
Output signal rise time	TR_output_CT	-	10	ns/V	

10.7 Connectivity Test Mode Timing Test Load

For ODT timing, refer to the reference load definition in Figure 23.

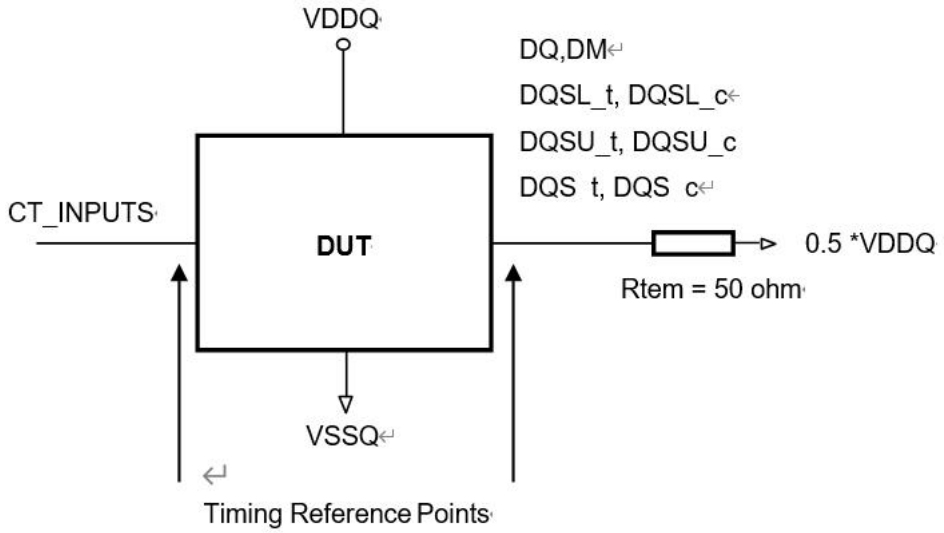


Figure 23 Connectivity Test Mode Timing Reference Load

11. DDR Speed Grades

Table 49 DDR4-1600 Speed Grades

Speed Parameters				DDR4	-1600		
CL-nRCD-nRP				11-1	1-11	Unit	Notes
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA		18.00	ns	11
Internal read command with read DBI enabled to first data			tAA_DBI	tAA(min) + 2nCK	tAA(max) + 2nCK	ns	11
ACT to internal read or write delay time			tRCD		15.00	ns	11
PRE command period			tRP		15.00	ns	11
ACT to PRE command period			tRAS	35	9 x tREFI	ns	11
ACT to ACT or REF command period			tRC		-	ns	11
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 10
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1, 2, 3, 10
CWL = 9, 11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1, 2, 3, 4, 11
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1, 2, 3, 6
CWL =10, 12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1, 2, 3, 4, 6
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1, 2, 3, 6

CWL =11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,6
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,6
CWL =12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,6
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,6
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
Supported CL Settings				10, (11), 12,(13),14,(15),16,(17),18		nCK	12
Supported CL Settings with Read DBI				12, (13), 14,(15),17,(18),19,(20),21		nCK	
Supported CWL Settings				9, 10, 11, 12 , 14, 16		nCK	

Table 50 DDR4-1866 Speed Grade

Speed Grade			DDR4-1866			
CL-nRCD-nRP			13-13-13		Unit	Notes
Parameter		Symbol	Min	Max		
Internal read command to first data		tAA		18.00	ns	11
Internal read command with read DBI enabled to first data		tAA_DBI	tAA(min) + 2nCK	tAA(max) + 2nCK	ns	11
ACT to internal read or write delay time		tRCD		15.00	ns	11
PRE command period		tRP		15.00	ns	11
ACT to PRE command period		tRAS	34	9 x tREFI	ns	11
ACT to ACT or REF command period		tRC		-	ns	11
	General	Read DBI				
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved	ns	1,2,3,4,10
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,11
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL =10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,6
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,6

CWL =11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,6
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,6
CWL =12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,6
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,6
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
Supported CL Settings				10, (11), 12,(13),14,(15),16,(17),18		nCK	12
Supported CL Settings with Read DBI				12, (13), 14,(15),17,(18),19,(20),21		nCK	
Supported CWL Settings				9, 10, 11, 12 , 14, 16		nCK	

Table 51 – DDR4-2133 Speed Grade

Speed Grade			DDR4-2133			
CL-nRCD-nRP			15-15-15		Unit	Notes
Parameter		Symbol	Min	Max		
Internal read command to first data		tAA		18.00	ns	11
Internal read command with read DBI enabled to first data		tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	11
ACT to internal read or write delay time		tRCD		15.00	ns	11
PRE command period		tRP		15.00	ns	11
ACT to PRE command period		tRAS	33	9 x tREFI	ns	11
ACT to ACT or REF command period		tRC		-	ns	11
	General	Read DBI				
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved	ns	1,2,3,4,10
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,11
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL =10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4

	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,6
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,6
CWL =11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,6
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,6
CWL =12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,6
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,6
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
Supported CL Settings				10, (11), 12,(13),14,(15),16,(17),18		nCK	12
Supported CL Settings with Read DBI				12, (13), 14,(15),17,(18),19,(20),21		nCK	
Supported CWL Settings				9, 10, 11, 12 , 14, 16		nCK	

Table 52: DDR4-2400 Speed Grade

Speed Grade			DDR4-2400			
CL-nRCD-nRP			17-17-17		Unit	NOTE
Parameter		Symbol	Min	Max		
Internal read command to first data		tAA		18.00	ns	11
Internal read command with read DBI enabled to first data		tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	11
ACT to internal read or write delay time		tRCD	14.16	-	ns	11
PRE command period		tRP	14.16	-	ns	11
ACT to PRE command period		tRAS	32	9 x tREFI	ns	11
ACT to ACT or REF command period		tRC	46.16	-	ns	11
	General	Read DBI				
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved	ns	1,2,3,4,10
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	4

	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,11
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL =10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,6
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,6
CWL =11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,6
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,6
CWL =12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,6
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,6
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
Supported CL Settings				10, (11), 12,(13),14,(15),16,(17),18		nCK	12
Supported CL Settings with Read DBI				12, (13), 14,(15),17,(18),19,(20),21		nCK	
Supported CWL Settings				9, 10, 11, 12 , 14, 16		nCK	

Table 53: DDR4-2666 Speed Grades

Speed Grade		DDR4-2666		Unit	Notes
CL-nRCD-nRP		19-19-19			
Parameter	Symbol	Min	Max		
Internal read command to first data	tAA		18.00	ns	11
Internal read command with read DBI enabled to first data	tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	11
ACT to internal read or write delay time	tRCD	14.25	-	ns	11
PRE command period	tRP	14.25	-	ns	11

ACT to PRE command period			tRAS	32	9 x tREFI	ns	11
ACT to ACT or REF command period			tRC	46.25	-	ns	11
	General	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 10
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1, 2, 3, 10
CWL = 9, 11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1, 2, 3, 4, 11
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1, 2, 3, 7
CWL =10, 12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1, 2, 3, 4, 7
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1, 2, 3, 7
CWL =11, 14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1, 2, 3, 4, 7
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1, 2, 3, 7
CWL =12, 16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 7
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1, 2, 3, 4, 7
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1, 2, 3
CWL =14, 18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1, 2, 3, 4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1, 2, 3, 4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1, 2, 3, 4
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1, 2, 3
Supported CL Settings				10, (11), 12, (13), 14, (15), 16, (17), 18, 19, 20		nCK	12
Supported CL Settings with Read DBI				12, (13), 14, (15), 17, (18), 19, (20), 21, 22, 23		nCK	
Supported CWL Settings				9, 10, 11, 12 , 14, 16, 18		nCK	

Table 54: DDR4-2933 Speed Grade

Speed Grade	**DDR4-2933**		
CL-nRCD-nRP	**21-21-21**	**Unit**	**Notes**

Parameter			Symbol	Min	Max		
Internal read command to first data			tAA		18.00	ns	11
Internal read command with read DBI enabled to first data			tAA_DBI	tAA(min) + 4nCK	tAA(max) + 4nCK	ns	11
ACT to internal read or write delay time			tRCD	14.32	-	ns	11
PRE command period			tRP	14.32	-	ns	11
ACT to PRE command period			tRAS	32	9 x tREFI	ns	11
ACT to ACT or REF command period			tRC	46.32	-	ns	11
	General	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 8, 10
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1, 2, 3, 8, 10
CWL = 9, 11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 8
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1, 2, 3, 4, 8, 12
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1, 2, 3, 8.14
CWL =10, 12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 8
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1, 2, 3, 4, 8, 14
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1, 2, 3, 8, 14
CWL =11, 14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 8
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1, 2, 3, 4, 8, 14
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1, 2, 3, 8, 14
CWL =12, 16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 8
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 8, 14
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1, 2, 3, 4, 8, 14
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1, 2, 3, 8, 14
	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 8

CWL =14, 18	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 8, 14
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1, 2, 3, 4, 8, 14
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1, 2, 3, 8, 14
CWL =16, 20	CL = 19	CL = 23	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 8
	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 8
	CL = 21	CL = 26	tCK(AVG)	0.682	<0.75	ns	1, 2, 3, 4, 8
	CL = 22	CL = 26	tCK(AVG)	0.682	<0.75	ns	1, 2, 3
Supported CL Settings				10, (11), 12, (13), 14, (15), 16, (17), 18, (19), 20, 21, 22		nCK	12
Supported CL Settings with Read DBI				12, (13), 14, (15), 16, (18), 19, (20), 21, (22), 23, 25, 26		nCK	12
Supported CWL Settings				9, 10, 11, 12 , 14, 15, 16, 18, 20		nCK	

Table 36: DDR4-3200 Speed Grade

Speed Grade			DDR4-3200		Unit	Notes
CL-nRCD-nRP			22-22-22			
Parameter		Symbol	Min	Max		
Internal read command to first data		tAA	13.75	18.00	ns	11
Internal read command with read DBI enabled to first data		tAA_DBI	tAA(min) + 4nCK	tAA(max) + 4nCK	ns	11
ACT to internal read or write delay time		tRCD	13.75	-	ns	11
PRE command period		tRP	13.75	-	ns	11
ACT to PRE command period		tRAS	32	9 x tREFI	ns	11
ACT to ACT or REF command period		tRC	45.75	-	ns	11
	General	Read DBI				
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved	ns	1, 2, 3, 4, 10
	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	1, 2, 3, 4, 10

CWL = 9, 11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1, 2, 3, 4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1, 2, 3, 4, 9
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1, 2, 3, 9
CWL =10, 12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1, 2, 3, 4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1, 2, 3, 4, 9
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1, 2, 3, 9
CWL =11, 14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1, 2, 3, 4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1, 2, 3, 4, 9
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1, 2, 3, 9
CWL =12, 16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1, 2, 3, 4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 9
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1, 2, 3, 4, 9
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1, 2, 3, 9
CWL =14, 18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1, 2, 3, 4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1, 2, 3, 4, 9
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1, 2, 3, 4, 9
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1, 2, 3.9
CWL =16, 20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1, 2, 3, 4
	CL = 22	CL = 26	tCK(AVG)	0.625	<0.75	ns	1, 2, 3, 4
	CL = 24	CL = 28	tCK(AVG)	0.625	<0.75	ns	1, 2, 3
Supported CL Settings				10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 24		nCK	1, 2
Supported CL Settings with Read DBI				12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, 24, 26, 28		nCK	
Supported CWL Settings				9, 10, 11, 12 , 14, 16, 18, 20		nCK	

11.1 Speed Grade Table Notes

Absolute Specifications

- VDDQ = VDD = 1.20v +/- 0.06 v

- VPP = 2.5v +0.25/-0.125 v

— Values defined in the table above are for DLL enabled state

1. The tCK(avg) MIN and tCK(avg) MAX requirements are derived from the CL setting and CWL setting. When selecting tCK(avg), both CL and CWL setting requirements must be met.

2. tCK(avg) MIN limitation: Since CAS latency is not purely analog - data and strobe outputs are synchronized by

DLL - not all possible intermediate frequencies are guaranteed. CL in the clock period is calculated from tAA using the rounding algorithm defined in Section 14.5.

3. tCK(avg) MAX limitation: Calculate tCK(avg) = tAA MAX / CL(selected), and round the resulting tCK(avg) to the next valid speed bin (i.e., 1.5ns, 1.25ns, 1.071ns, 0.937ns, or 0.833ns). This result is the tCK(avg) MAX corresponding to the selected CL.
4. "Reserved" settings are not allowed. The user must program a different value.
5. "Optional" settings allow some devices in the industry to support this setting, but it is not a mandatory feature. Refer to the vendor's datasheet and/or DIMM SPD information for details on whether and how this setting is supported.
6. Any DDR4-2400 speed bin also supports functional operation at the lower frequencies shown in the table. These frequencies are not subject to production test, but are verified by design/characterization.
7. Any DDR4-2666 speed bin also supports functional operation at the lower frequencies shown in the table. These frequencies are not subject to production test, but are verified by design/characterization.
8. Any DDR4-2933 speed bin also supports functional operation at the lower frequencies shown in the table. These frequencies are not subject to production test, but are verified by design/characterization.
9. Any DDR4-3200 speed bin also supports functional operation at the lower frequencies shown in the table. These frequencies are not subject to production test, but are verified by design/characterization.
10. DDR4-1600 AC timing applies for DRAM operation at data rates lower than 1600 MT/s.
11. Parameters from tCK(avg) MIN to tCK(avg) MAX apply to all standard JEDEC clock period values as described in the speed bin table.
12. CL numbers in parentheses indicate that these values are optional.
13. DDR4 SDRAM supports CL=9 as long as the system meets tAA(min).
14. For a given DRAM to comply with JEDEC standards, the timing requirements that must be supported are listed for each speed bin. JEDEC compliance does not require supporting all speed bins within a given speed grade. JEDEC compliance requires meeting the parameters of at least one listed speed bin.

12. IDD and IDDQ Specifications and Test Conditions

12.1 IDD, IPP, and IDDQ Measurement Conditions

In this section, IDD, IPP, and IDDQ measurement conditions such as test load and patterns are defined. Figure 24 shows the setup and test load for IDD, IPP, and IDDQ measurements.

- Standard IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA,

IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7, and IDD8) are measured as time-averaged currents with all VDD pins of the DUT DDR4 SDRAM tied together. Any IPP or IDDQ currents are not included in IDD currents.

- IPP currents have the same definition as IDD, except that the current is measured on the VPP supply.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ pins of the DUT DDR4 SDRAM tied together. Any IDD currents are not included in IDDQ currents. Note: IDDQ values cannot be used directly to calculate the I/O power consumption of the DDR4 SDRAM. They may be used to support correlation of simulated I/O power versus actual I/O power, as shown in Figure 25. In DRAM module applications, IDDQ cannot be measured separately because VDD and VDDQ share a combined power plane on the module PCB.

The definitions for IDD, IPP, and IDDQ measurements are as follows:

- "0" and "LOW" are defined as VIN <= VILAC(max).
- "1" and "HIGH" are defined as VIN >= VIHAC(min).
- "MID-LEVEL" is defined as the input being VREF = VDD / 2.
- Timing for IDD, IPP, and IDDQ measurement loop patterns is shown in Table 56.
- The basic IDD, IPP, and IDDQ measurement conditions are shown in Table 57. A detailed description of IDD, IPP, and IDDQ measurement loop patterns.
- Tables 58 through 66 list the conditions for IDD measurements after proper initialization of the DDR4 SDRAM, including but not limited to the settings:
- RON = RZQ/7 (34 Ω in MR1); RTT_NOM = RZQ/6 (40 Ω in MR1); RTT_WR = RZQ/2 (120 Ω in MR2);
- RTT_PARK = Disabled;
- In MR1, Qoff = B (output buffer enabled); TDQS_t disabled in MR1;
- CRC disabled in MR2;
- CA parity function disabled in MR5; read/write DBI disabled in MR5; DM disabled in MR5;
- Note: Before starting actual IDD or IDDQ measurements, the IDD, IPP, and IDDQ measurement loop patterns must be executed at least once.
- Define D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} = {HIGH, LOW, LOW, LOW, LOW}; apply BG/BA changes when indicated.
- Define D# = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} = {HIGH, HIGH, HIGH, HIGH, HIGH}; apply the inverse of BG/BA changes when indicated above.

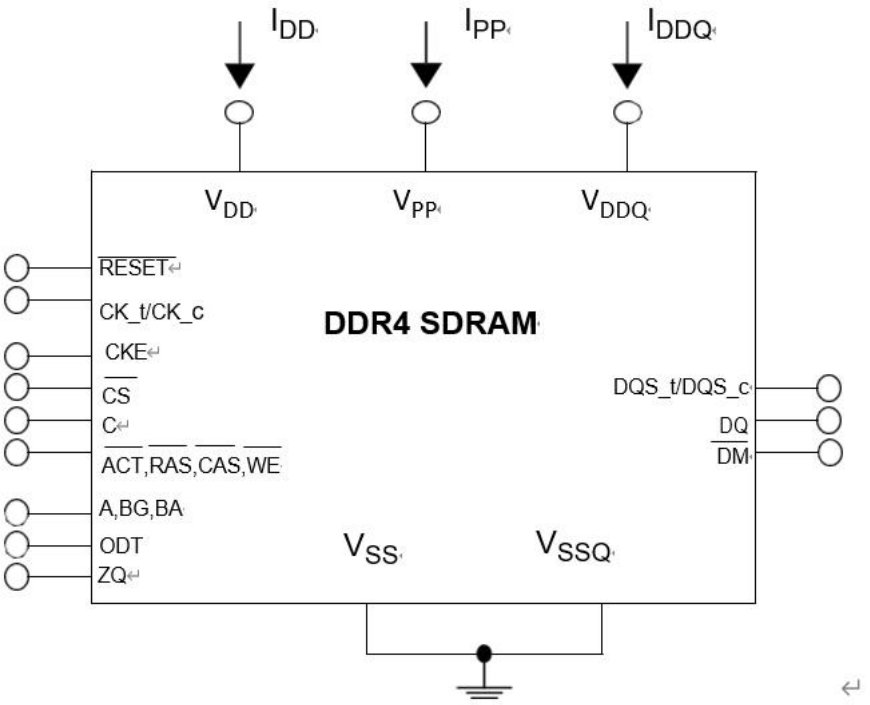


Figure 24: Measurement Setup and Test Load for IDD, IPP, and IDDQ Measurements

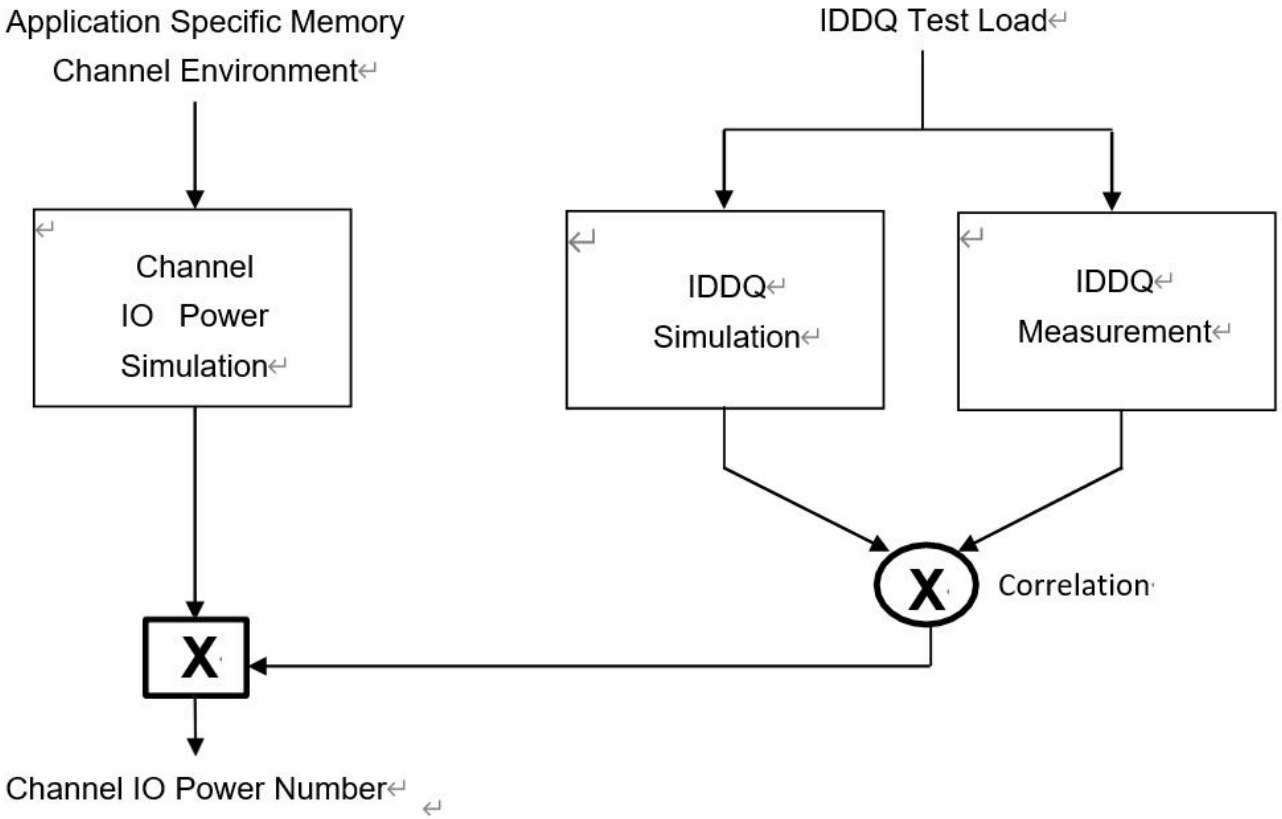


Figure 25 Correlation between IDDQ measurement supported analog channel IO power and actual channel IO power.

Table 56 Loop Mode Timing for IDD, IPP, and IDDQ Measurements

Symbol	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
	17-17-17	19-19-19	21-21-21	22-22-22	

tCK		0.833	0.75	0.682	0.625	ns
CL		17	19	21	22	nCK
CWL		14	18	18	20	nCK
nRCD		17	19	21	22	nCK
nRC		56	62	67	74	nCK
nRAS		39	43	47	52	nCK
nRP		17	19	21	22	nCK
nFAW	x4	16	16	16	16	nCK
	x8	26	28	31	34	nCK
	x16	36	40	44	48	nCK
nRRDS	x4	4	4	4	4	nCK
	x8	4	4	4	4	nCK
	x16	7	7	8	9	nCK
nRRDL	x4	6	7	8	8	nCK
	x8	6	7	8	8	nCK
	x16	8	9	10	11	nCK
tCCD_S		4	4	4	4	nCK
tCCD_L		6	7	8	8	nCK
tWTR_S		3	4	4	4	nCK
tWTR_L		9	10	11	12	nCK
nRFC 2Gb		193	214	235	256	nCK
nRFC 4Gb		313	347	382	416	nCK
nRFC 8Gb		421	467	514	560	nCK
TBD						nCK

Table 57 Basic IDD, IPP, and IDDQ Measurement Conditions

Symbol	Description

IDD0	Operating One Bank Active-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, CL: See Table 56, BL: 8; AL: 0; CS_n: High between ACT and PRE commands; Command, Address, Bank Group Address, Bank Address: toggling according to Table 58 Data I/O: VDDQ; DM_n: Held at 1; Bank Activation: only one bank active at a time: 0,0,1,1,2,2,... (see Table 54) Output Buffer and RTT: enabled in Mode Register 2; ODT Signal: held at 0; Mode details: as per Table 58
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, other conditions: see IDD0
IPP0	Operating One Bank Active-Precharge IPP Current Same conditions as IDD0
IDD1	Operating One Bank Active-Read-Precharge (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: as per Table 52; AL: 0; CS_n: HIGH during ACT, RD, and PRE commands; Command, Address, Bank Group, Bank Address, Data IO: toggling as per Table 55 DM_n: held at 1;

	Bank Activity: only one bank at a time: 0,0,1,1,2,2,... (as per Table 55); Output buffer and RTT: enabled in mode registers; ODT Signal: held LOW; Mode details: as per Table 58
IDD1A	Operating one bank Active-Read-Precharge current (AL=CL-1) AL = CL-1, all other conditions: as per IDD1
IPP1	Operating One Bank Active-Read-Precharge IPP Current Same conditions as IDD1
IDD2N	Precharge Standby Current (AL=0) CKE: High; External clock: On; tCK, CL: See Table 52; BL: 8; AL: 0; CS_n: Held at 1; Command, address, bank group address, bank address: Toggling according to Table 60; Data IO: VDDQ; DM_n: held at 1; Bank Activity: All banks closed; Output buffer and RTT: Enabled in Mode Register 2; ODT Signal: held at 0; Mode details: See Table 60;
IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, other conditions: see IDD2N
IPP2N	Precharge Standby IPP Current Same conditions as IDD2N

IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 57; AL: 0; CS_n: Held at 1; Command, Address, Bank Group, Bank Address: toggling according to Table 57; Data IO: VSSQ; DM_n: Held at 1; Bank Activity: All banks closed; Output buffer and RTT: enabled in mode registers; ODT Signal: toggling according to Table 61; Mode details: see Table 61
IDDQ2NT (Optional)	Precharge Standby ODT IDDQ Current Same definition as IDD2NT, but measures IDDQ current instead of IDD current.
IDD2NL	Precharge Standby Current with CAL enabled. Same definition as IDD2N and CAL.
IDD2NG	Precharge Standby Current with Gear Down Mode enabled. Same definition as IDD2N and Gear Down Mode.
IDD2ND	Precharge Standby Current with DLL disabled. Same definition as IDD2N and DLL.
IDD2N_par	Precharge Standby Current with CA parity enabled. Same definition as IDD2N and CA parity.
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 56 AL: 0; CS_n: Held at 1;

	Command, Address, Bank Group Address, Bank Address: held at 0; Data IO: VDDQ; DM_n: held at 1; Bank Activity: All banks closed; Output Buffer and RTT: Disabled ODT Signal: Static to 0
IPP2P	Precharge Power-Down IPP Current Same conditions as IDD2P
IDD2Q	Precharge Quiet Standby Current CKE: high; External clock: ON; tCK, CL: See Table 56; BL: 8; AL: 0; CS_n: Held at 1; Command, Address, Bank Group Address, Bank Address: held at 0; Data IO: VDDQ; DM_n: held at 1; Bank Activity: All Banks Closed; Output Buffer and RTT: Enabled in Mode Register; ODT Signal: Static to 0
IDD3N	Active Standby Current CKE: High; External clock: enabled; tCK, CL: as in Table 56; BL: 8[1];

	AL: 0; CS_n: held at 1; Command, Address, Bank Group Address, Bank Address: toggled according to Table 56 Data IO: VDDQ; DM_n: held at 1; Bank Activity: All Banks Open; Output Buffer and RTT: Enabled in Mode Register; ODT Signal: Held at 0; Mode details: See Table 60
IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, other conditions: see IDD3N
IPP3N	Active Standby IPP Current Same conditions as IDD3N
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: See Table 56; AL: 0; CS_n: Held at 1; Command, Address, Bank Group Address, Bank Address: Held at 0; Data IO: VDDQ; DM_n: held at 1; Bank Activity: All Banks Active Output Buffer and RTT: Enabled in mode registers; ODT Signal: Static to 0
IPP3P	Active Power-Down IPP Current Same conditions as IDD3P
	Operating Burst Read Current

IDD4R	CKE: High; External clock: On; tCK, CL: see Table 56; AL: 0; CS_n: Low during RD; Command, Address, Bank Group, Bank Address: Toggling according to Table 58; Data IO: Continuous read bursts, data different between bursts, as shown in Table 62; DM_n: held at 1; Bank Activity: All banks open, RD command cycling through banks: 0,0,1,1,2,2,... (see Table 62); Output buffer and RTT: enabled in mode registers; ODT Signal: held at 0; Pattern details: see Table 62
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, other conditions: see IDD4R
IDD4RB	Read DBI condition, Operating Burst Read Current Read DBI, other conditions: see IDD4R
IPP4R	Operating Burst Read IPP Current Same conditions as IDD4R
IDDQ4R (Optional)	Operating Burst Read IDDQ Current Same definition as IDD4R, but measures IDDQ current instead of IDD current
IDDQ4RB (Optional)	Read DBI condition, Operating Burst Read IDDQ Current Same definition as IDD4RB, but measures IDDQ current instead of IDD current
IDD4W	Operating Burst Write Current CKE: high; External clock: enabled; tCK, CL: see Table 56; AL: 0; CS_n: High during WR;

	Command, Address, Bank Group Address, Bank Address: toggle according to Table 63 Data IO: seamless write burst, data different between bursts, as shown in Table 63; DM_n: held at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 63); Output buffer and RTT: enabled in mode registers; ODT Signal: held high Mode details: see Table 63
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, other conditions: see IDD4W
IDD4WB	Under write DBI condition, Operating Burst Write Current With Write DBI, other conditions: see IDD4W
IDD4WC	With Write CRC, Operating Burst Write Current With Write CRC, other conditions: see IDD4W
IDD4W_par	With CA Parity, Operating Burst Write Current With CA Parity, other conditions: see IDD4W
IPP4W	Operating Burst Write IPP Current Same conditions as IDD4W
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: see Table 56; AL: 0; CS_n: HIGH during REF; Command, Address, Bank Group Address, Bank Address: toggling according to Table 65 Data IO: VDDQ; DM_n: held at 1; Bank Activity: REF command executed each nRFC (see Table 65); Output Buffer and RTT: Enabled in mode register; ODT Signal: held at 0;

	Mode details: see Table 65
IPP5B	Burst Refresh Write IPP Current (1X REF) Same conditions as IDD5B
IDD5F2	Burst Refresh Current (2X REF) tRFC = tRFC_x2, other conditions: see IDD5B
IPP5F2	Burst Refresh Write IPP Current (2X REF) Same conditions as IDD5F2
IDD5F4	Burst Refresh Current (4X REF) tRFC = tRFC_x4, other conditions: see IDD5B
IPP5F4	Burst Refresh Write IPP Current (4X REF) Same conditions as IDD5F4
IDD6N	Self Refresh Current: Normal Temperature Range: 0 - 85° C; Low Power Auto SelfRefresh (LP ASR) : CKE: Low; External clock: Off; CK_t and CK_c: Low; CL: See Table 56; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: held at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Register; ODT Signal: MID-LEVEL
IPP6N	Self Refresh IPP Current: Normal Temperature Range Same conditions as IDD6N
IDD6E	Self-Refresh Current: Extended Temperature Range : 0 - 95° C; Low Power Auto Self Refresh (LP ASR) : CKE: Low; External clock: Off; CK_t and CK_c#: Low;

	CL: See Table 56 AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: held at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in mode register; ODT Signal: MID-LEVEL
IPP6E	Self Refresh IPP Current: Extended Temperature Range Same conditions as IDD6E
IDD6R	Self-Refresh Current: Reduced Temperature Range: 0 - 45 ° C; Low Power Auto Self Refresh (LP ASR) : CKE: Low; External clock: Off; CK_t and CK_c#: Low; CL: See Table 56 AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: Stay at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in mode register; ODT Signal: MID-LEVEL
IPP6R	Self Refresh IPP Current: Reduced Temperature Range Same conditions as IDD6R
IDD6A	Auto Self-Refresh Current: Extended Temperature Range : 0 - 95° C; Low Power Auto Self Refresh (LP ASR) : CKE: Low; External clock: Off; CK_t and CK_c: Low; CL: See Table 56; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data I/O: High; DM_n: Held at 1; Bank Activity: Auto Self-Refresh Operation; Output Buffer and RTT: Enabled in Mode Register; ODT Signal: MID-LEVEL
	Auto Self-Refresh IPP Current

IPP6A	Same conditions as IDD6A
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: See Table 56; AL: CL-1; CS_n, command, address, bank group address, bank address, Data IO: toggling according to Table 66 Data IO: read burst with different data patterns according to Table 62; DM_n: held at 1; Bank Activity: two interleaved cycles through different addressed banks (0, 1, ... 7), see Table 66; Output Buffer and RTT: enabled in mode registers ODT Signal: held at 0; Mode details: see Table 66
IPP7	Operating Bank Interleave Read IPP Current Same conditions as IDD7
IDD8	Maximum Power Down Current TBD
IPP8	Maximum Power Down IPP Current Same conditions as IDD8

Note:

1. Burst length: BL8 fixed by MRS; set MR0[A1:A0] = 00.

2. Output Buffer Enable

Set MR1[A12]=0 to enable output buffer (Qoff = 0).

- Set MR1 [A2:1 = 00]: Output Driver Impedance Control = RZQ/7

RTT_Nom Enable

- Set MR1 [A10:8 = 011]: RTT_NOM = RZQ/6

RTT_WR Enable

- Set MR2 [A10:9 = 01]: RTT_WR = RZQ/2

RTT_PARK Disable

- Set MR5 [A8:6 = 000]

3. CAL Enable: Set MR4 [A8:6 = 001]: 1600MT/s

MR4 [A8:6 = 010]: 1866MT/s, 2133MT/s

MR4 [A8:6 = 011]: 2400MT/s

Disable DLL: Set MR1 [A0 = 0]

CA Parity Enable: Set MR5 [A2:0 = 001]: 1600MT/s, 1866MT/s, 2133MT/s

MR5 [A2:0 = 010]: 2400MT/s

Read DBI Enable: Set MR5 [A12 = 1]; Write DBI Enable: Set MR5 [A11 = 1]

4. Low-Power Auto Self-Refresh (LP ASR): Set MR2 [A7:6 = 00]: Normal;

MR2 [A7:6 = 01]: Reduced Temperature Range

MR2 [A7:6 = 10]: Extended Temperature Range;

MR2 [A7:6 = 11]: Automatic Self-Refresh

5. IDD2N shall be measured after a NOP (No Operation) input.

Table 58: IDD0, IDD0A, and IPP0 Measurement Loop Pattern 1

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13, 11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	data
T	S		0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3.4	D_#, D_#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		0	…	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			…	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC	repeat Sub-Loop 0, use BG 1 0 [2]= 1, BA[1:0] = 1 instead																
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 2 instead																
		3	3*nRC	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 3 instead																
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0] = 0, BA[1:0] = 1 instead																

		5	5*nRC	repeat Sub-Loop 0, use BG[1:0] = 1, BA[1:0] = 2 instead	
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0]=0, BA[1:0]=3 instead	
		7	7*nRC	repeat Sub-Loop 0, use BG[1:0]=1, BA[1:0]=0 instead	
		8	8*nRC	repeat Sub-Loop 0, use BG[1:0]=2, BA[1:0]=0 instead	For x4 and x8 only
		9	9*nRC	repeat Sub-Loop 0, use BG[1:0]=3, BA[1:0]=1 instead	
		10	10 C	repeat Sub-Loop 0, use BG=2, BA[1:0]=2 instead	
		11	11 C	repeat Sub-Loop 0, use BG=3, BA[1:0]=3 instead	
		12	12 C	repeat Sub-Loop 0, use BG=2, BA[1:0]=1 instead	
		13	13 C	repeat Sub-Loop 0, use BG=3, BA[1:0]=2 instead	
		14	14*nRC C	repeat Sub-Loop 0, use BG 1 0 [2]= 2, BA[1:0] = 3 instead	
		15	15*nRC C	repeat Sub-Loop 0, use BG 1 0 [2]= 3, BA[1:0] = 0 instead	

Note

1. DQS_t, DQS_c are at VDDQ.
2. BG1 can be ignored for x16 devices
3. C[2:0] is applicable only to 3DS devices
4. DQ signals are at VDDQ.

Table 59 IDD1, IDD1A and IPP1 Measurement Loop Patterns

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	data[4]
		0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3.4	D#, D#	1	1	1	1	1	0	0	3[b]	3	0	0	0	7	F	0	–
			…	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																
																				D0=00, D1=FF

		nRCD -AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
		...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																	
		nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	-
		...	repeat pattern 1...4 until nRC - 1, truncate if necessary																	
	1	1*nRC + 0	ACT	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	-
		1*nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		1*nRC + 3, 4	D#, D#	1	1	1	1	1	0	0	3^b	3	0	0	0	7	F	0	0	-
		...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																	
		1*nRC + nRCD - AL	RD	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
		...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																	
		1*nRC + nRAS	PRE	0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	-
		...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																	
	2	2*nRC	repeat Sub-Loop 0, use BG[1:0]=0, BA[1:0]=2 instead																	
	3	3*nRC	repeat Sub-Loop 1, use BG[1:0]=1, BA[1:0]=3 instead																	
	4	4*nRC	repeat Sub-Loop 0, use BG[1:0]=0, BA[1:0]=1 instead																	
	5	5*nRC	repeat Sub-Loop 1, use BG[1:0]=1, BA[1:0]=2 instead																	
	6	6*nRC	repeat Sub-Loop 0, use BG 1 0 ^{2}= 0, BA[1:0] = 3 instead																	
	8	7*nRC	repeat Sub-Loop 1, use BG 1 0 ^{2}= 1, BA[1:0] = 0 instead																	
	9	9*nRC	repeat Sub-Loop 1, use BG 1 0 ^{2}= 2, BA[1:0] = 0 instead																	
	10	10*nRC	repeat Sub-Loop 0, use BG 1 0 ^{2}= 3, BA[1:0] = 1 instead																	
	11	11*nRC	repeat Sub-Loop 1, use BG 1 0 ^{2}= 2, BA[1:0] = 2 instead																	
	12	12*nRC	repeat Sub-Loop 0, use BG 1 0 ^{2}= 3, BA[1:0] = 3 instead																	For x4 and
	13	13*nRC	repeat Sub-Loop 1, use BG = 1, BA[1:0] = 1 instead																	x8 only
	14	14*nRC	repeat Sub-Loop 0, use BG 1 0 ^{2}= 3, BA[1:0] = 2 instead																	
	15	15*nRC	repeat Sub-Loop 1, use BG = 1, BA[1:0] = 3 instead																	
	16	16*nRC	repeat Sub-Loop 0, use BG 1 0 ^{2}= 3, BA[1:0] = 0 instead																	

Note

1. DQS_t, DQS_c are toggled with RD commands; otherwise at VDDQ.

2. BG1 is don't care for x16 devices

3. C[2:0] is applicable only to 3DS devices

4. The burst sequence on each DQ signal is driven by a read command. Outside burst operation, DQ signals are at VDDQ.

Table 60 IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2, IDD3N, IDD3NA and IDD3P Measurement Loop Patterns

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	data[4]
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	2, 2	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	0
			3	D#, D#	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	0
		1	4-7	repeat Sub-Loop 0, use BG[1:0]=01, BA[1:0]=1 instead																
		2	8-11	repeat Sub-Loop 0, use BG[1:0]=00, BA[1:0]=2 instead																
		3	12-15	repeat Sub-Loop 0, use BG[1:0]=01, BA[1:0]=3 instead																
		4	16-19	repeat Sub-Loop 0, use BG[1:0]=00, BA[1:0]=1 instead																
		5	20-23	repeat Sub-Loop 0, use BG[1:0]=01, BA[1:0]=2 instead																
		6	24-27	repeat Sub-Loop 0, use BG[1:0]=00, BA[1:0]=3 instead																
		7	28-31	repeat Sub-Loop 0, use BG[1:0]=1, BA[1:0]=0 instead																
		8	32-35	repeat Sub-Loop 0, use BG[1:0]=2, BA[1:0]=0 instead																
		9	36-39	repeat Sub-Loop 0, use BG 1 0 ^{2} = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, use BG[1:0]=2, BA[1:0]=2 instead																
		11	44-47	repeat Sub-Loop 0, use BG[1:0]=3, BA[1:0]=3 instead																
		12	48-51	repeat Sub-Loop 0, use BG[1:0]=2, BA[1:0]=1 instead																
		13	52-55	repeat Sub-Loop 0, use BG[1:0]=3, BA[1:0]=2 instead																
		14	56-59	repeat Sub-Loop 0, use BG[1:0]=2, BA[1:0]=3 instead																
		15	60-63	repeat Sub-Loop 0, use BG 1 0 ^{2} = 3, BA[1:0] = 0 instead																

Note

1. DQS_t, DQS_c are at VDDQ.

2. BG1 is don't care for x16 devices

3. C[2:0] is applicable only to 3DS devices

4. DQ signals are at VDDQ.

Table 61 IDD2NT and IDDQ2NT Measurement Loop Pattern

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13, 11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	data[4]
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			2	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	–
			3	D#, D#	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	–
		1	4–7	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 1 instead																
		2	8–11	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 0, BA[1:0] = 2 instead																
		3	12–15	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 3 instead																
		4	16–19	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 0, BA[1:0] = 1 instead																
		5	20–23	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 2 instead																
		6	24–27	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 0, BA[1:0] = 3 instead																
		7	28–31	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 1, BA[1:0] = 0 instead																
		8	32–35	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 0 instead																For x4 and x8 only
		9	36–39	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 1 instead																
		10	40–43	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 2 instead																
		11	44–47	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 3 instead																
		12	48–51	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 1 instead																
		13	52–55	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 2 instead																
		14	56–59	repeat Sub-Loop 0, but ODT = 0 and BG[1:0] = 2, BA[1:0] = 3 instead																
		15	60–63	repeat Sub-Loop 0, but ODT = 1 and BG[1:0] = 3, BA[1:0] = 0 instead																

Note

1. DQS_t, DQS_c are at VDDQ.

2. BG1 is don't care for x16 devices

3. C[2:0] is applicable only to 3DS devices

4. DQ signals are at VDDQ.

Table 62 IDD4R, IDD4RA, IDD4RB, and IDDQ4R Measurement Loop Pattern

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	data[4]	
Toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF	
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–	
			2.3	D#, D#	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	–	
		1	4	RD	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00	
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–	
			6,7	D#, D#	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	–	
		2	8–11	repeat Sub-Loop 0, use BG 1 0 [2] = 0, BA[1:0] = 2 instead																	
		3	12–15	repeat Sub-Loop 1, use BG 1 0 [2] = 1, BA[1:0] = 3 instead																	
		4	16–19	repeat Sub-Loop 0, use BG 1 0 [2] = 0, BA[1:0] = 1 instead																	
		5	20–23	repeat Sub-Loop 1, use BG 1 0 [2] = 1, BA[1:0] = 2 instead																	
		6	24–27	repeat Sub-Loop 0, use BG 1 0 [2] = 0, BA[1:0] = 3 instead																	
		7	28–31	repeat Sub-Loop 1, use BG 1 0 [2] = 1, BA[1:0] = 0 instead																	
		8	32–35	repeat Sub-Loop 0, use BG 1 0 [2] = 2, BA[1:0] = 0 instead																	For x4 and x8 only
		9	36–39	repeat Sub-Loop 1, use BG 1 0 [2] = 3, BA[1:0] = 1 instead																	
		10	40–43	repeat Sub-Loop 0, use BG 1 0 [2] = 2, BA[1:0] = 2 instead																	
		11	44–47	repeat Sub-Loop 1, use BG 1 0 [2] = 3, BA[1:0] = 3 instead																	
		12	48–51	repeat Sub-Loop 0, use BG 1 0 [2] = 2, BA[1:0] = 1 instead																	
		13	52–55	repeat Sub-Loop 1, use BG 1 0 [2] = 3, BA[1:0] = 2 instead																	
		14	56–59	repeat Sub-Loop 0, use BG 1 0 [2] = 2, BA[1:0] = 3 instead																	
		15	60–63	repeat Sub-Loop 1, use BG 1 0 [2] = 3, BA[1:0] = 0 instead																	

Note

1. DQS_t, DQS_c are used with RD commands; otherwise, they are at VDDQ.
2. BG1 is don't care for x16 devices
3. C[2:0] is applicable only to 3DS devices
4. Burst sequence driven on each DQ signal by a read command.

Table 63: IDD4W, IDD4WA, IDD4WB, and IDD4W_par Measurement Loop Patterns

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	data[4]
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			2, 3	D#, D#	1	1	1	1	1	1	0	3^2	3	0	0	0	7	F	0	-
		1	4	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			6, 7	D#, D#	1	1	1	1	1	1	0	3^2	3	0	0	0	7	F	0	-
		2	8–11	repeat Sub-Loop 0, use BG 1 0 [2] = 0, BA[1:0] = 2 instead																
		3	12–15	repeat Sub-Loop 1, use BG 1 0 [2] = 1, BA[1:0] = 3 instead																
		4	16–19	repeat Sub-Loop 0, use BG 1 0 [2] = 0, BA[1:0] = 1 instead																
		5	20–23	repeat Sub-Loop 1, use BG 1 0 [2] = 1, BA[1:0] = 2 instead																
		6	24–27	repeat Sub-Loop 0, use BG 1 0 [2] = 0, BA[1:0] = 3 instead																
		7	28–31	repeat Sub-Loop 1, use BG 1 0 [2] = 1, BA[1:0] = 0 instead																
		8	32–35	repeat Sub-Loop 0, use BG 1 0 [2] = 2, BA[1:0] = 0 instead																
		9	36–39	repeat Sub-Loop 1, use BG 1 0 [2] = 3, BA[1:0] = 1 instead																
		10	40–43	repeat Sub-Loop 0, use BG 1 0 [2] = 2, BA[1:0] = 2 instead																

11	44–47	repeat Sub-Loop 1, use BG 1 0 [2] = 3, BA[1:0] = 3 instead	For x4 and x8 only
12	48–51	repeat Sub-Loop 0, use BG 1 0 [2] = 2, BA[1:0] = 1 instead	
13	52–55	repeat Sub-Loop 1, use BG 1 0 [2] = 3, BA[1:0] = 2 instead	
14	56–59	repeat Sub-Loop 0, use BG 1 0 [2] = 2, BA[1:0] = 3 instead	
15	60–63	repeat Sub-Loop 1, use BG 1 0 [2] = 3, BA[1:0] = 0 instead	

Note

1. DQS_t, DQS_c are used per WR command; otherwise, they are at VDDQ
2. BG1 is don't care for x16 devices
3. C[2:0] is applicable only to 3DS devices
4. Write command drives burst sequence on each DQ signal.

Table 64: IDD4WC Measurement Loop Pattern

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	data[4]
T	S	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC
			1,2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		1	5	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC
			6,7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			8,9	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		2	10–14	repeat Sub-Loop 0, use BG 1 0 [2] = 0, BA[1:0] = 2 instead																
		3	15–19	repeat Sub-Loop 1, use BG 1 0 [2] = 1, BA[1:0] = 3 instead																

		4	20-24	repeat Sub-Loop 0, use BG 1 0 ^{2} = 0, BA[1:0] = 1 instead	
		5	25-29	repeat Sub-Loop 1, use BG 1 0 ^{2} = 1, BA[1:0] = 2 instead	
		6	30-34	repeat Sub-Loop 0, use BG 1 0 ^{2} = 0, BA[1:0] = 3 instead	
		7	35-39	repeat Sub-Loop 1, use BG 1 0 ^{2} = 1, BA[1:0] = 0 instead	
		8	40-44	repeat Sub-Loop 0, use BG 1 0 ^{2} = 2, BA[1:0] = 0 instead	For x4 and x8 only
		9	45-49	repeat Sub-Loop 1, use BG 1 0 ^{2} = 3, BA[1:0] = 1 instead	
		10	50-54	repeat Sub-Loop 0, use BG 1 0 ^{2} = 2, BA[1:0] = 2 instead	
		11	55-59	repeat Sub-Loop 1, use BG 1 0 ^{2} = 3, BA[1:0] = 3 instead	
		12	60-64	repeat Sub-Loop 0, use BG 1 0 ^{2} = 2, BA[1:0] = 1 instead	
		13	65-69	repeat Sub-Loop 1, use BG 1 0 ^{2} = 3, BA[1:0] = 2 instead	
		14	70-74	repeat Sub-Loop 0, use BG 1 0 ^{2} = 2, BA[1:0] = 3 instead	
		15	75-79	repeat Sub-Loop 1, use BG 1 0 ^{2} = 3, BA[1:0] = 0 instead	

Note

1. DQS_t, DQS_c are at VDDQ
2. BG1 is don't care for x16 devices
3. C[2:0] is applicable only to 3DS devices
4. Burst sequence is driven on each DQ signal by the write command.

Table 65: IDD5B Measurement Loop Pattern

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0]^{3}	BG[1:0]^{2}	BA[1:0]	A12/BC_n	A[13, 11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	data^{4}
T	S	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D#, D#	1	1	1	1	1	0	0	3^{2}	3	0	0	0	7	F	0	-
			4	D#, D#	1	1	1	1	1	0	0	3^{2}	3	0	0	0	7	F	0	-
			4-7	repeat pattern 1...4, use BG 1 0 ^{2} = 1, BA[1:0] = 1 instead																
			8-11	repeat pattern 1...4, use BG 1 0 ^{2} = 0, BA[1:0] = 2 instead																
			12-15	repeat pattern 1...4, use BG 1 0 ^{2} = 1, BA[1:0] = 3 instead																
			16-19	repeat pattern 1...4, use BG 1 0 ^{2} = 0, BA[1:0] = 1 instead																

		1	20–23	repeat pattern 1...4, use BG 1 0 [2] = 1, BA[1:0] = 2 instead	
			24–27	repeat pattern 1...4, use BG[1:0] = 0, BA[1:0] = 3 instead	
			28–31	repeat pattern 1...4, use BG[1:0] = 1, BA[1:0] = 0 instead	
			32–35	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 0 instead	For x4 and x8 only
			36–39	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 1 instead	
			40–43	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 2 instead	
			44–47	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 3 instead	
			48–51	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 1 instead	
			52–55	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 2 instead	
			56–59	repeat pattern 1...4, use BG[1:0] = 2, BA[1:0] = 3 instead	
			60–63	repeat pattern 1...4, use BG[1:0] = 3, BA[1:0] = 0 instead	
		2	64 ... nRFC – 1	repeat Sub-Loop 1, Truncate, if necessary	

Note

1. DQS_t, DQS_c are at VDDQ
2. BG1 is don't care for x16 devices
3. C[2:0] is applicable only to 3DS devices
4. DQ signals are placed at VDDQ level.

Table 66: IDD7 Measurement Loop Pattern

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[3, 11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	data[4]
		0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1	RDA	0	1	1	0	1	0		0	0	0	0	1	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	–
			...	repeat pattern 2...3 until nRRD – 1, if nRRD > 4. Truncate if necessary																
		1	nRRD	ACT	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	–

			nRRD + 1	RDA	0	1	1	0	1	0		1	1	0	0	1	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			...	repeat pattern 2...3 until 2*nRRD - 1, if nRRD > 4. Truncate if necessary																
		2	2*nRRD	repeat Sub-Loop 0, use BG 1 0 ^{2} = 0, BA[1:0] = 2 instead																
		3	3*nRRD	repeat Sub-Loop 1, use BG 1 0 ^{2} = 1, BA[1:0] = 3 instead																
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRRD. Truncate if necessary																
		5	nFAW	repeat Sub-Loop 0, use BG 1 0 ^{2} = 0, BA[1:0] = 1 instead																
		6	nFAW+ nRRD	repeat Sub-Loop 1, use BG 1 0 ^{2} = 1, BA[1:0] = 2 instead																
		7	nFAW+2*nRRD	repeat Sub-Loop 0, use BG 1 0 ^{2} = 0, BA[1:0] = 3 instead																
		8	nFAW+3*nRRD	repeat Sub-Loop 1, use BG 1 0 ^{2} = 1, BA[1:0] = 0 instead																
		9	nFAW+4*nRRD	nFAW+4*nRRD																
		10	2*nFAW	repeat Sub-Loop 0, use BG 1 0 ^{2} = 2, BA[1:0] = 0 instead																For x4 and x8 only
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use BG 1 0 ^{2} = 3, BA[1:0] = 1 instead																
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG 1 0 ^{2} = 2, BA[1:0] = 2 instead																
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG 1 0 ^{2} = 3, BA[1:0] = 3 instead																
		14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																
		15	3*nFAW	repeat Sub-Loop 0, use BG 1 0 ^{2} = 2, BA[1:0] = 1 instead																
		16	3*nFAW + nRRD	repeat Sub-Loop 1, use BG 1 0 ^{2} = 3, BA[1:0] = 2 instead																
		17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG 1 0 ^{2} = 2, BA[1:0] = 3 instead																
		18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG 1 0 ^{2} = 3, BA[1:0] = 0 instead																
		19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																
		20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																

Note

1. DQS_t, DQS_c are at VDDQ
2. BG1 is don't care for x16 devices
3. C[2:0] is applicable only to 3DS devices
4. The burst sequence on each DQ signal is driven by a read command. Outside burst operation, DQ signals are at VDDQ.

12.2 IDD Specifications

Unless otherwise noted, IDD and IPP values apply to the full operating range of voltage and temperature.

Table 67 IDD and IDDQ Specification Example 1

Parameter	1G x 8				Unit	Notes
	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200		
	17-17-17	19-19-19	21-21-21	22-22-22		
	IDD Max.	IDD Max.	IDD Max.	IDD Max.		
I_{DD0}	71	79	84	100	mA	
I_{DD0A}	72	80	85	101	mA	
I_{DD1}	101	104	114	145	mA	
I_{DD1A}	101	104	114	145	mA	
I_{DD2N}	50	60	70	81	mA	
I_{DD2NA}	51	61	71	82	mA	
I_{DD2NT}	85	89	94	99	mA	
I_{DD2NL}	50	60	70	81	mA	
I_{DD2NG}	49	59	69	80	mA	
I_{DD2ND}	40	50	60	70	mA	
I_{DD2N_PAR}	85	89	94	99	mA	
I_{DD2P}	45	50	65	76	mA	
I_{DD2Q}	40	50	61	71	mA	
I_{DD3N}	81	90	101	112	mA	
I_{DD3NA}	82	91	102	113	mA	
I_{DD3P}	77	80	92	108	mA	
I_{DD4R}	211	231	255	275	mA	
I_{DD4RA}	211	231	255	275	mA	
I_{DD4RB}	212	232	256	276	mA	
I_{DD4W}	178	230	268	285	mA	
I_{DD4WA}	178	230	268	285	mA	
I_{DD4WB}	178	230	268	285	mA	
I_{DD4WC}	190	252	288	305	mA	
I_{DD4W_PAR}	210	263	298	325	mA	
I_{DD5B}	267	299	299	300	mA	
I_{DD5F2}	224	224	224	264	mA	
I_{DD5F4}	200	200	200	226	mA	
I_{DD6N}	25	25	25	25	mA	

I_{DD6E}	35	35	35	35	mA	
I_{DD6R}	20	20	20	20	mA	
I_{DD6A}	22	22	22	22	mA	
I_{DD7}	256	268	289	326	mA	
I_{DD8}	23	23	23	23	mA	

Table 67 (Continued)

Parameter	512M x16				Unit	Notes
	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200		
	17-17-17	19-19-19	21-21-21	22-22-22		
	IDD Max.	IDD Max.	IDD Max.	IDD Max.		
I_{DD0}	81	89	94	111	mA	
I_{DD0A}	82	90	93	112	mA	
I_{DD1}	110	114	124	159	mA	
I_{DD1A}	111	115	125	160	mA	
I_{DD2N}	50	60	70	81	mA	
I_{DD2NA}	51	61	71	82	mA	
I_{DD2NT}	85	89	94	99	mA	
I_{DD2NL}	50	60	70	81	mA	
I_{DD2NG}	49	59	69	80	mA	
I_{DD2ND}	40	50	60	70	mA	
I_{DD2N_PAR}	85	89	94	99	mA	
I_{DD2P}	45	50	65	76	mA	
I_{DD2Q}	40	50	61	71	mA	
I_{DD3N}	81	90	101	112	mA	
I_{DD3NA}	82	91	102	113	mA	
I_{DD3P}	77	80	92	108	mA	
I_{DD4R}	271	296	321	359	mA	
I_{DD4RA}	275	300	325	365	mA	
I_{DD4RB}	271	296	321	359	mA	
I_{DD4W}	248	265	280	314	mA	
I_{DD4WA}	248	265	280	314	mA	
I_{DD4WB}	250	270	281	316	mA	
I_{DD4WC}	260	280	291	326	mA	
I_{DD4W_PAR}	275	295	306	341	mA	

I_{DD5B}	267	299	299	300	mA	
I_{DD5F2}	224	224	224	264	mA	
I_{DD5F4}	200	200	200	226	mA	
I_{DD6N}	25	25	25	25	mA	
I_{DD6E}	35	35	35	35	mA	
I_{DD6R}	20	20	20	20	mA	
I_{DD6A}	22	22	22	22	mA	
I_{DD7}	358	368	388	420	mA	
I_{DD8}	23	23	23	23	mA	

Table 68: IDD Specifications (continued)

Parameter	1G x 8				Unit	Notes
	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200		
	17-17-17	19-19-19	21-21-21	22-22-22		
	IPP Max.	IPP Max.	IPP Max.	IPP Max.		
I_{PP0}	7	7	7	7	mA	
I_{PP1}	7	7	7	7	mA	
I_{PP2N}	3.5	3.5	3.5	3.5	mA	
I_{PP2P}	3.5	3.5	3.5	3.5	mA	
I_{PP3N}	4	4	4	4	mA	
I_{PP3P}	4	4	4	4	mA	
I_{PP4R}	4	4	4	4	mA	
I_{PP4W}	4	4	4	4	mA	
I_{PP5B}	37	37	37	37	mA	
I_{PP5B_F2}	28	28	28	28	mA	
I_{PP5B_F4}	22	22	22	22	mA	
I_{PP6N}	4	4	4	4	mA	
I_{PP6E}	4	4	4	4	mA	
I_{PP7}	28	28	28	28	mA	
I_{PP8}	4	4	4	4	mA	

Continued Table 68

Parameter	512M x 16				Unit	Notes
	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200		
	17-17-17	19-19-19	21-21-21	22-22-22		

	IPP Max.	IPP Max.	IPP Max.	IPP Max.		
I_{PP0}	7	7	7	7	mA	
I_{PP1}	7	7	7	7	mA	
I_{PP2N}	3.5	3.5	3.5	3.5	mA	
I_{PP2P}	3.5	3.5	3.5	3.5	mA	
I_{PP3N}	4	4	4	4	mA	
I_{PP3P}	4	4	4	4	mA	
I_{PP4R}	4	4	4	4	mA	
I_{PP4W}	4	4	4	4	mA	
I_{PP5B}	37	37	37	37	mA	
I_{PP5B_F2}	28	28	28	28	mA	
I_{PP5B_F4}	22	22	22	22	mA	
I_{PP6N}	4	4	4	4	mA	
I_{PP6E}	4	4	4	4	mA	
I_{PP7}	28	28	28	28	mA	
I_{PP8}	4	4	4	4	mA	

Table 69 IDD6 Specification

Parameter	Temperature Range	1G x 8				Unit	Notes
		2400	2666	2933	3200		
		17-17-17	19-19-19	21-21-21	22-22-22		
I_{DD6N}	0 - 85°C	25	25	25	25	mA	3
I_{DD6E}	0 - 95°C	35	35	35	35	mA	4
I_{DD6R}	0 - 45°C	20	20	20	20	mA	5
I_{DD6A}	0 - 95°C	22	22	22	22	mA	6

Continued Table 69

Parameter	Temperature Range	512M x 16				Unit	Notes
		2400	2666	2933	3200		
		17-17-17	19-19-19	21-21-21	22-22-22		

I_{DD6N}	0 – 85°C	25	25	25	25	mA	3
I_{DD6E}	0 – 95°C	35	35	35	35	mA	4
I_{DD6R}	0 – 45°C	20	20	20	20	mA	5
I_{DD6A}	0 – 95°C	22	22	22	22	mA	6

Note

1. For x16 organization, some IDD currents are higher due to the larger page size architecture.
2. Maximum IDD current values consider the worst-case process, temperature, and voltage.
3. Applies for MR2 settings A6=0 and A7=0.
4. Applies for MR2 settings A6=0, A7=1. IDD6E applies only to devices supporting extended temperature range.
5. Applies for MR2 settings A6=1, A7=0. IDD6A is specified only for devices supporting automatic self-refresh.
6. The number of supported discrete temperature ranges and associated Ta-Tz values are supplier/design specific. All supported TOPER values specify the temperature range.
7. Applies for MR2 settings A6=1 and A7=0: reduced temperature range. IDD6R is design and characterization verified, may not require production test.

13. I/O Capacitance

Table 70 Silicon Substrate I/O Capacitance

Symbol	Parameter	DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
C_{IO}	I/O Capacitance	0.55	1.15	0.55	1.15	0.55	1.00	0.55	1.00	pF	1, 2, 3
C_{DIO}	I/O Capacitance Delta	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1, 2, 3, 11
C_{DDQS}	I/O Capacitance Delta DQS_t and DQS_c	–	0.05	–	0.05	–	0.05	–	0.05	pF	1, 2, 3, 5
C_{CK}	Input Capacitance CK_t and CK_c	0.2	0.7	0.2	0.7	0.2	0.7	0.2	0.7	pF	1, 3
C_{DCK}	Input Capacitance Delta CK_t and CK_c	–	0.05	–	0.05	–	0.05	–	0.05	pF	1, 3, 4

C_I	Input Capacitance (CTRL, ADD, CMD Pins))	0.2	0.7	0.2	0.7	0.2	0.6	0.2	0.55	pF	1,3,6
C_{DI_CTRL}	Input Capacitance Delta (All CTRL Pins))	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
$C_{DI_ADD_CMD}$	Input Capacitance Delta (All ADD/CMD Pins)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C_{ALERT}	ALERT I/O Capacitance	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	pF	1,3
C_{ZQ}	ZQ I/O Capacitance	-	2.3	-	2.3	-	2.3	-	2.3	pF	1,3,12
C_{TEN}	TEN Input Capacitance	0.2	2.3	0.2	2.3	0.2	2.3	0.2	2.3	pF	1,3,13

Note

1. This parameter is not production tested. It is verified by design and characterization. Verification of pure silicon capacitance by de-embedding package L and C parasitics. Capacitance measured with VDD, VDDQ, VSS, VSSQ applied and all other signal pins floating. Measurement procedure TBD.
2. DQ, DM_n, DQS_T, DQS_C, TDQS_T, TDQS_C. DM, TDQS_T, and TDQS_C pins, though functionally different, are load matched to DQ and DQS.
3. This parameter applies only to single-die devices; stacked/dual-die devices are not included here.
4. Absolute value of CK_T - CK_C.
5. Absolute value of CIO(DQS_T) - CIO(DQS_C).
6. CI applies to ODT, CS_n, CKE, A0-A16, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n, and PAR.
7. CDI_CTRL applies to ODT, CS_n, and CKE.
8. $C_{DI_CTRL} = C_I$ (ctrl)-0.5*(C_I (CLK_t) + C_I (CLK _c))。
9. CDI_ADD_CMD applies to A0-A16, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n, and PAR.

10. $C_{DI_ADD_CMD}$ = C_I (ADD_CMD) -0.5 * (C_I (CLK_T) + C_I (CLK_C))。

11. C_{DIO} = C_{IO}(DQ, DM)-0.5*(C_{IO} (DQS_t)+ cio (DQS_c))。

12. Maximum external load capacitance on ZQ pin: TBD pF.

13. The TEN pin is internally pulled low through a weak pull-down resistor to VSS. In this case, CTEN may be invalid. The system should verify the TEN signal according to vendor-specific information.

Table 71: DRAM Package Electrical Specifications (x8)

Symbol	Parameter	1Gbx8								Unit	Notes
		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200			
		Min	Max	Min	Max	Min	Max	Min	Max		
Z_{IO}	Input/output Zpkg	45	85	45	85	48	85	48	85	W	1, 2, 4, 5, 10, 11
Td_{IO}	Input/output Pkg Delay	14	42	14	42	14	40	14	40	ps	1, 3, 4, 5, 11
L_{IO}	Input/Output Lpkg	-	3.3	-	3.3	-	3.3	-	3.3	nH	11, 12
C_{IO}	Input/Output Cpkg	-	0.78	-	0.78	-	0.78	-	0.78	pF	11, 13
Z_{IO_DQS}	DQS_t, DQS_c Zpkg	45	85	45	85	48	85	48	85	W	1, 2, 5, 10, 11
Td_{IO_DQS}	DQS_t, DQS_c Pkg Delay	14	42	14	42	14	40	14	40	ps	1, 3, 5, 10, 11
L_{IO_DQS}	DQS Lpkg	-	3.3	-	3.3	-	3.3	-	3.3	nH	11, 12
C_{IO_DQS}	DQS Cpkg	-	0.78	-	0.78	-	0.78	-	0.78	pF	11, 13
DZIO_DQS	Delta Zpkg DQS_t, DQS_c	-	10	-	10	-	10	-	10	W	1, 2, 5, 7, 10
D_{TDIO_DQS}	Delta Delay DQS_t, DQS_c	-	5	-	5	-	5	-	5	ps	1, 3, 5, 7, 10
Z_{I_CTRL}	Input- CTRL pins Zpkg	50	90	50	90	50	90	50	90	W	1, 2, 5, 9, 10, 11
T_{DI_CTRL}	Input- CTRL pins Pkg Delay	14	42	14	42	14	40	14	40	ps	1, 3, 5, 9, 10, 11
L_{I_CTRL}	Input CTRL Lpkg	-	3.4	-	3.4	-	3.4	-	3.4	nH	11, 12
C_{I_CTRL}	Input CTRL Cpkg	-	0.7	-	0.7	-	0.7	-	0.7	pF	11, 13
Z_{IADD_CTRL}	Input- CMD ADD pins Zpkg	50	90	50	90	50	90	50	90	W	1, 2, 5, 8, 10, 11

Td_{IADD_CTRL}	Input- CMD ADD pins Pkg Delay	14	45	14	45	14	40	14	40	ps	1, 3, 5, 8, 10, 11
L_{IADD_CTRL}	Input CMD ADD Lpkg	–	3.6	–	3.6	–	3.6	–	3.6	nH	11, 12
C_{IADD_CTRL}	Input CMD ADD Cpkg	–	0.74	–	0.74	–	0.74	–	0.74	pF	11, 13
Z_{CK}	CLK_t & CLK_c Zpkg	50	90	50	90	50	90	50	90	W	1, 2, 5, 10, 11
TD_{CK}	CLK_t & CLK_c Pkg Delay	14	42	14	42	14	42	14	42	ps	1, 3, 5, 10, 11
L_{I_CK}	Input CLK Lpkg	–	3.4	–	3.4	–	3.4	–	3.4	nH	11, 12
C_{I_CK}	Input CLK Cpkg	–	0.7	–	0.7	–	0.7	–	0.7	pF	11, 13
DZ_{DCK}	Delta Zpkg CLK_t & CLK_c	–	10	–	10	–	10	–	10	W	1, 2, 5, 6, 10
Td_{DCK}	Delta Delay CLK_t & CLK_c	–	5	–	5	–	5	–	5	ps	1, 3, 5, 6, 10
Z_{OZQ}	ZQ Zpkg	–	100	–	100	–	100	–	100	W	1, 2, 5, 10, 11
Td_{OZQ}	ZQ Delay	20	90	20	90	20	90	20	90	ps	1, 3, 5, 10, 11
Z_{O_ALERT}	ALERT Zpkg	40	100	40	100	40	100	40	100	W	1, 2, 5, 10, 11
Td_{O_ALERT}	ALERT Delay	20	55	20	55	20	55	20	55	ps	1, 3, 5, 10, 11

Note

1. This parameter is not production tested. It is verified by design and characterization. Package parasitics (L and C) are verified using package samples only. Capacitance is measured with VDD, VDDQ, VSS, VSSQ shorted and all other signal pins floating. Inductance is measured with VDD, VDDQ, VSS, and VSSQ shorted and all other signal pins shorted at the die side (not at the pins). Measurement procedure is TBD.
2. Package impedance (Zpkg) is calculated from the total Lpkg and Cpkg of the given pin: Zpkg = sqrt(Lpkg / Cpkg).

$$= \sqrt{Lpkg/Cpkg}$$

3. Package delay (Tpkg) is calculated from the total Lpkg and Cpkg of the given pin: Tpkg = sqrt(Lpkg * Cpkg).

$$= \sqrt{Lpkg\ Cpkg}$$

4. Z and Td apply to DQ, DM, TDQS_T, and TDQS_C.
5. This parameter applies only to single-die devices; stacked/dual-die devices are not included here.
6. Absolute value of impedance ZCK_t - ZCK_c (Z) or absolute value of delay TdCK_t - TdCK_c (Td).

7. Absolute value of ZIO(DQS_t) - ZIO(DQS_c) for impedance (Z) or absolute value of TdIO(DQS_t) - TdIO(DQS_c) for delay (Td).
8. ZI and Td ADD CMD apply to A0-A13, ACT_n, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, and PAR.
9. ZI and Td CTRL apply to ODT, CS_n, and CKE.
10. This table applies to single-die X8 devices.
11. If Zpkg and Pkg delay fall within the shown range and the maximum Lpkg and Cpkg do not exceed the shown maximum values, the package implementation shall comply with the specification.
12. Assume Lpkg can be approximated as Lpkg = Zo * Td.
13. Assume Cpkg can be approximated as Cpkg = Td / Zo.

Table 72 DRAM Package Electrical Specifications (x16)

Symbol	Parameter	512Mx16		Unit	Notes
		DDR4-2400 to DDR4-3200			
		Min	Max		
Z_{IO}	Input/output Zpkg	45	85	W	1
Td_{IO}	Input/output Pkg Delay	14	45	ps	1
L_{IO}	Input/Output Lpkg	-	3.4	nH	1,2
C_{IO}	Input/Output Cpkg	-	0.82	pF	1,3
Z_{IO_DQS}	DQS_t, DQS_c Zpkg	45	85	W	1
Td_{IO_DQS}	DQS_t, DQS_c Pkg Delay	14	45	ps	1
L_{IO_DQS}	DQS Lpkg	-	3.4	nH	1,2
C_{IO_DQS}	DQS Cpkg	-	0.82	pF	1,3
DZ_{dIO_DQS}	Delta Zpkg DQSU_t, DQSU_c	-	10	W	-
	Delta Zpkg DQSL_t, DQSL_c	-	10	W	-
D_{TDIO_DQS}	Delta Delay DQSU_t, DQSU_c	-	5	ps	-
	Delta Delay DQSL_t, DQSL_c	-	5	ps	-
Z_{I_CTRL}	Input CTRL pins Zpkg	50	90	W	1
T_{DI_CTRL}	Input CTRL pins Pkg Delay	14	42	ps	1
L_{I_CTRL}	Input CTRL Lpkg	-	3.4	nH	1,2
C_{I_CTRL}	Input CTRL Cpkg	-	0.7	pF	1,3
Z_{IADD_CTRL}	Input- CMD ADD pins Zpkg	50	90	W	1
Td_{IADD_CTRL}	Input- CMD ADD pins Pkg Delay	14	52	ps	1

L_{IADD_CTRL}	Input CMD ADD Lpkg	–	3.9	nH	1,2
C_{IADD_CTRL}	Input CMD ADD Cpkg	–	0.86	pF	1,3
Z_{CK}	CLK_c Zpkg	50	90	W	1
TD_{CK}	CLK_c Pkg Delay	14	42	ps	1
L_{I_CK}	Input CLK Lpkg	–	3.4	nH	1,2
C_{I_CK}	Input CLK Cpkg	–	0.7	pF	1,3
DZ_{DCK}	Delta Zpkg CLK_c	–	10	W	–
Td_{DCK}	Delta Delay CLK_c	–	5	ps	–
Z_{OZQ}	ZQ Zpkg	–	100	W	–
Td_{OZQ}	ZQ Delay	20	90	ps	–
Z_{O_ALERT}	ALERT Zpkg	40	100	W	–
Td_{O_ALERT}	ALERT Delay	20	55	ps	–

Note

1. If Zpkg and Pkg delay fall within the shown range and the maximum Lpkg and Cpkg do not exceed the shown maximum values, the package implementation shall comply with the specification.
2. Assume Lpkg can be approximated as Lpkg = Zo * Td
3. Assume Cpkg can be approximated as Cpkg = Td / Zo

14. Electrical Characteristics and AC Timing

14.1 AC Timing and Output Slew Rate with Reference Load

Figure 26 shows a 50-ohm effective reference load used to define the related AC timing parameters and output voltage slew rate measurements of the device.

The nominal Ron of DQ, DQS_t, and DQS_c drivers is 34 ohms to specify the relevant AC timing parameters of the device.

Maximum DC high level of output signal = 1.0 * VDDQ,

Minimum DC low level of output signal = {34 / (34 + 50)} * VDDQ = 0.4 * VDDQ

The nominal reference level of the output signal can be approximately expressed as:

Center of maximum DC high level and minimum DC low level = {(1 + 0.4) / 2} * VDDQ = 0.7 * VDDQ

The actual reference level of the output signal may vary with driver Ron and reference load tolerances. Therefore, the actual reference level or midpoint of the output signal is located at the widest part of the output signal eye. Before measuring AC parameters, the reference level of the verification tool should be set to an appropriate level. It is not intended to be an exact representation of any specific system environment, nor is it intended as a description

of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load with the system environment. Manufacturers correlate with their production test conditions, typically one or more coaxial transmission lines terminated at the tester electronics.

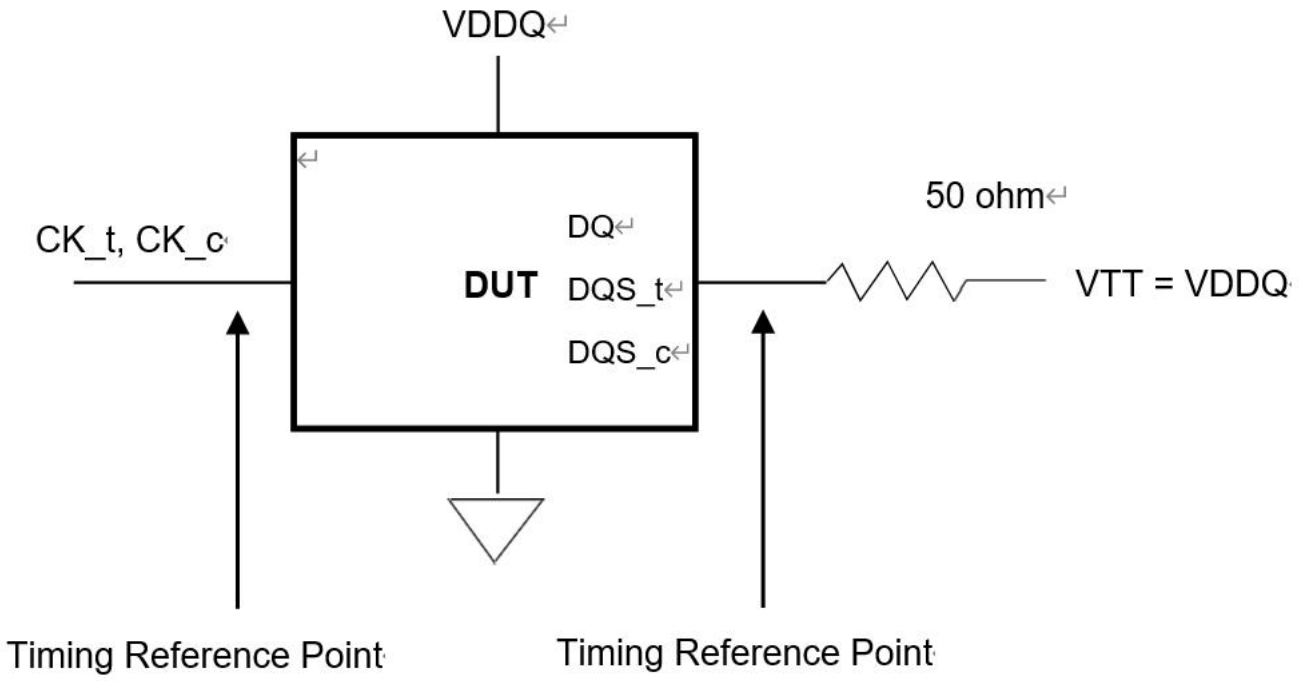


Figure 26: AC Timing and Output Slew Rate Testing with Reference Load

14.2 tREFI

The average periodic refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table

Table 73: tREFI vs. Density

Parameter	Symbol		4Gb	8Gb	Symbol	Notes
Average Refresh Interval	tREFI	0°C≦TCASE≦85°C	7.8	7.8	us	
		-40°C≦TCASE≦85°C	7.8	7.8	us	1
		85°C<TCASE≦95°C	3.9	3.9	us	

Note:

Supports industrial temperature only

14.3 CLK Specification

Specified jitter is random jitter that conforms to Gaussian distribution. Violating the min/max values of the input clock may cause the DDR4 SDRAM device to malfunction.

14.3.1 Definition of tCK(abs)

tCK(abs) is defined as the absolute clock period, measured from one rising edge to the next consecutive rising edge.

tCK(abs) is not subject to production test constraints.

14.3.2 Definition of tCK(avg)

tCK(avg) is calculated as the average clock period over any consecutive 200-cycle window, where each clock period is measured from rising edge to rising edge.

14.3.3 Definition of tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, calculated over any consecutive 200 high pulses.

tCL(avg) is defined as the average low pulse width, calculated over any consecutive 200 low pulses.

14.3.4 Definition of tERR(nper)

tERR is defined as the cumulative error over n consecutive cycles of n × tCK(avg). tERR is not constrained by production testing.

14.4 Timing Parameters by Speed Grade

Table 74 Timing Parameters for DDR4-1600 to DDR4-2133 Speed Grades

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Minimum Clock Cycle Time (DLL Off Mode)	tCK(DLL_OFF)	8	20	8	20	8	20	ns	-
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.937	<1.071	ns	35, 36
Average High Pulse Width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average Low Pulse Width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min = tCK(avg)min + tJIT(per)min_tot Max = tCK(avg)max + tJIT(per)max_tot						tCK(avg)	
Absolute Clock High Pulse Width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute Clock Low Pulse Width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter - Total	JIT(per)_tot	-63	63	-54	54	-47	47	ps	23

Clock Period Jitter - Deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	ps	26
Clock Period Jitter during DLL Locking	tJIT(per, lck)	-50	50	-43	43	-38	38	ps	
Cycle to Cycle Jitter	tJIT(cc)	-	125	-	107	-	94	ps	
Cycle to Cycle Jitter during DLL Locking	tJIT(cc, lck)	-	100	-	86	-	75	ps	
Cumulative Error across 2 Cycles	tERR(2per)	-92	92	-79	79	-69	69	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	ps	
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	ps	
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	ps	
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	ps	
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	ps	
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	ps	
Cumulative error across 15 periods	tERR(15per)	-178	178	-152	152	-133	133	ps	
Cumulative error across 16 periods	tERR(16per)	-180	180	-155	155	-135	135	ps	

Cumulative error across 17 periods	tERR(17per)	-183	183	-157	157	-137	137	ps	
Cumulative error across 18 periods	tERR(18per)	-185	185	-159	159	-139	139	ps	
Cumulative error across n = 13, 14 ... 49, 50 periods	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)						ps	
Command and Address Setup Time to CK_t, CK_c Refer to Vih(ac) / Vil(ac) standard	tIS(base)	115	-	100	-	80	-	ps	
Command and Address Setup Time to CK_t, CK_c Refer to Vref standard	tIS(Vref)	215	-	200	-	180	-	ps	
Command and Address Hold Time to CK_t, CK_c Refer to Vih(dc) / Vil(dc) standard	tIH(base)	140	-	125	-	105	-	ps	
Command and Address Hold Time to CK_t, CK_c Reference to Vref standard	tIH(Vref)	215	-	200	-	180	-	ps	

Table 74 continued

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Control and Address Input	tIPW								-

Pulse Width (per input)		600	–	525	–	460	–	ps	
CAS_n to CAS_n Command Delay for Same Bank Group	tCCD_L	Max (5nCK, 6. 250ns)	–	Max (5nCK, 6. 250ns)	–	Max (5nCK, 6. 250 ns)	–	nCK	34
CAS_n to CAS_n Command Delay for Different Bank Groups	tCCD_S	4	–	4	–	4	–	nCK	34
ACTIVATE to ACTIVATE Command Delay for Different Bank Groups (2KB Page Size)	tRRD_S(2K)	Max (4nCK, 6ns)	–	Max (4nCK, 5. 3ns)	–	Max (4nCK, 5. 3ns)	–	nCK	34
1KB Page Size, Different Bank Group Activate-to-Activate Command Delay	tRRD_S(1K)	Max (4nCK, 5ns)	–	Max (4nCK, 4. 2ns)	–	Max (4nCK, 3. 7ns)	–	nCK	34
Activate to activate command delay for different bank groups (1/2KB page size)	tRRD_S(1/2 K)	Max (4nCK, 5ns)	–	Max (4nCK, 4. 2ns)	–	Max (4nCK, 3. 7ns)	–	nCK	34
2KB page size, ACTIVATE-to-ACTIVATE command delay within the same bank group	tRRD_L(2K)	Max (4nCK, 7. 5ns)	–	Max (4nCK, 6. 4ns)	–	Max (4nCK, 6. 4ns)	–	nCK	34
1KB page size, ACTIVATE-to-ACTIVATE command delay within the same bank group	tRRD_L(1K)	Max (4nCK, 6ns)	–	Max (4nCK, 5. 3ns)	–	Max (4nCK, 5. 3ns)	–	nCK	34
1/2KB page size, ACTIVATE-to-ACTIVATE command delay within the same bank group	tRRD_L (1/2K)	Max (4nCK, 6ns)	–	Max (4nCK, 5. 3ns)	–	Max (4nCK, 5. 3ns)	–	nCK	34
Four activate windows (2KB page size)	tFAW_2K	Max (28nCK, 35 ns)	–	Max (28nCK, 30 ns)	–	Max (28nCK, 30 ns)	–	ns	34
Four activate windows (1KB page size)	tFAW_1K	Max (20nCK, 25 ns)	–	Max (20nCK, 23 ns)	–	Max (20nCK, 21 ns)	–	ns	34
Four activate windows (1/2KB page size)	tFAW_1/2K	Max (16nCK, 20ns)	–	Max (16nCK, 17ns)	–	Max (16nCK, 15ns)	–	ns	34
Internal write transaction to internal read command delay	tWTR_S	Max (2nCK,	–	max (2nCK,	–	Max (2nCK,	–	ns	1, 2, 34

within the same bank group		2.5ns)		2.5ns)		2.5ns)			
Internal write transaction to internal read command delay for a different bank group	tWTR_L	Max(4nCK, 7.5ns)	–	Max(4nCK, 7.5ns)	–	Max(4nCK, 7.5ns)	–	ns	1, 34
Internal read command to precharge command delay	tRTP	Max(4nCK, 7.5ns)	–	Max(4nCK, 7.5ns)	–	Max(4nCK, 7.5ns)	–	ns	34
Write recovery time	tWR	15	–	15	–	15	–	ns	1
Write recovery time with CRC and DM enabled	tWR_CRC_DM	tWR+max(4nCK, 3.75ns)	–	tWR+max(5nCK, 3.75ns)	–	tWR+max(5nCK, 3.75ns)	–	ns	1, 28
Write to read command delay for same bank group with CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max(4nCK, 3.75ns)	–	tWTR_S+max(5nCK, 3.75ns)	–	tWTR_S+max(5nCK, 3.75ns)	–	ns	2, 29, 34
Write to read command delay for same bank group with CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max(4nCK, 3.75ns)	–	tWTR_L+max(4nCK, 3.75ns)	–	tWTR_L+max(5nCK, 3.75ns)	–	ns	3, 30, 34
DLL locking time	tDLLK	597	–	597	–	768	–	nCK	
Mode Register Set command cycle time	tMRD	8	–	8	–	8	–	nCK	
Mode Register Set command update delay	tMOD	Max(24nCK, 15ns)	–	Max(24nCK, 15ns)	–	Max(24nCK, 15ns)	–	nCK	50
Multi-Purpose Register recovery time	tMPRR	1	–	1	–	1	–	nCK	33
Multi-Purpose Register write recovery time	tWR_MPR	tMOD(min)+ AL + PL	–	tMOD(min)+ AL + PL	–	tMOD(min)+ AL + PL	–	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))						nCK	

DQ0 or DQ1 driven to 0 setup time to first DQS rising edge	tPDA_S	0.5	–	0.5	–	0.5	–	UI	45, 47
DQ0 or DQ1 driven to 0 hold time from last DQS falling edge	tPDA_H	0.5	–	0.5	–	0.5	–	UI	46, 47
CS_n to command address delay	tCAL	Max (3nCK, 3.748 ns)	–	Max (3nCK, 3.748 ns)	–	Max (3nCK, 3.748 ns)	–	nCK	
Mode Register Set command cycle time in CAL mode	tMRD_tCAL	tMOD+tCAL	–	tMOD+tCAL	–	tMOD+tCAL	–	nCK	
Update delay in CAL mode of mode register setting	tMOD_tCAL	tMOD+tCAL	–	tMOD+tCAL	–	tMOD+tCAL	–	nCK	

Table 74 continued

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Per group, per access: DQS_t, DQS_c to DQ slew rate	tDQSQ	–	0.16	–	0.16	–	0.16	tCK(avg)/2	13, 18, 39, 49
Per access DQS_t, DQS_c, per group DQ output hold time	tQH	0.76	–	0.76	–	0.76	–	tCK(avg)/2	13, 17, 18, 39, 49
Data valid window per device per UI: (tQH – tDQSQ) per UI on a given DRAM	tDVWd	0.63	–	0.63	–	0.64	–	UI	17, 18, 39, 49
Data valid window per pin per UI: (tQH – tDQSQ) per UI on a given pin of a DRAM	tDVWp	0.66	–	0.66	–	0.69	–	UI	17, 18, 39, 49
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-450	225	-390	195	-360	180	ps	39
DQ high-impedance time from CK_t, CK_c	tHZ(DQ)	–	225	–	195	–	180	ps	39
DQS_t, DQS_c differential read preamble (1-clock preamble)	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	tCK	39, 40
DQS_t/DQS_c Differential Read Preamble (2-clock preamble)	tRPRE2	NA	NA	NA	NA	NA	NA	tCK	39, 41
DQS_t, DQS_c differential read postamble	tRPST	0.33	NOTE45	0.33	NOTE45	0.33	NOTE45	tCK	39
DQS_t, DQS_c differential output high time	tQSH	0.4	–	0.4	–	0.4	–	tCK	21, 39
DQS_t, DQS_c Differential Output Low Time	tQS	0.4	–	0.4	–	0.4	–	tCK	20, 39

	L								
DQS_t, DQS_c differential write preamble (1-clock preamble)	tWPRE	0.9	–	0.9	–	0.9	–	tCK	42
DQS_t, DQS_c differential write preamble (2-clock preamble)	tWPRE2	NA	–	NA	–	NA	–	tCK	43
DQS_t, DQS_c differential write postamble	tWPST	0.33	–	0.33	–	0.33	–	tCK	
DQS_t and DQS_c low-impedance time (refer to RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	ps	39
DQS_t and DQS_c high-impedance time (refer to RL+BL/2)	tHZ(DQS)	–	225	–	195	–	180	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c Differential Input High Pulse Width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c Rising Edge to CK_t, CK_c Rising Edge (1 Clock Preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c Rising Edge to CK_t, CK_c Rising Edge (2 Clock Preamble)	tDQSS2	–	–	–	–	–	–	tCK	43
DQS_t, DQS_c FalTing Edge Setup Time to CK_t, CK_c Rising Edge	tDSS	0.18	–	0.18	–	0.18	–	tCK	
DQS_t, DQS_c Falling Edge Hold Time to CK_t, CK_c Rising Edge	tDSH	0.18	–	0.18	–	0.18	–	tCK	
DQS_t, DQS_c rising edge output timing position relative to CK_t, CK_c rising edge (DLL enabled mode)	tDQSCK (DLL On)	-225	225	-195	195	-180	180	ps	37, 38, 39
DQS_t, DQS_c per DRAM Rising Edge Output Variance Window	tDQSCKI (DLL On)		370		330		310	ps	37, 38, 39
Command path delay to prohibit entry into MPSM	tMPED	Min = tMOD(min) + tCPDED(min)						nCK	
Valid Clock Requirement After MPSM Entry	tCKMPE	Min = tMOD(min) + tCPDED(min)						nCK	
Valid Clock Requirement Before MPSM Exit	tCKMPX	Min = tCKSRX (min)						nCK	
MPSM Exit to Command Not Requiring DLL Lock	tXMP	tXS(min)						nCK	
MPSM Exit to Command Requiring DLL Lock	tXMPDLL	Min = tXMP(min) + tXSDLL(min)						nCK	

CS_n setup time to CKE	tMPX_S	Min = tIS(min) + tIH(min)						ns	
CS_n high hold time to CKE rising edge	tMPX_HH	Min = tXP						ns	
CS_n low hold time to CKE rising edge	tMPX_IH	Min = 12; Max = tXMP-10ns						ns	
Power-up and reset calibration time	tZQinit	1024	–	1024	–	1024	–	nCK	
Normal operation full calibration time	tZQoper	512	–	512	–	512	–	nCK	
Normal operation short calibration time	tZQCS	128	–	128	–	128	–	nCK	

Table 74 continued

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
From CKE high to a valid command (Reset Exit)	tXPR	max(5nCK, tRFC(min)+10ns)	–	max(5nCK, tRFC(min)+10ns)	–	max(5nCK, tRFC(min)+10ns)	–	nCK	
Exit self refresh for commands not requiring a locked DLL	tXS	tRFC(min)+10ns	–	tRFC(min)+10ns	–	tRFC(min)+10ns	–	nCK	
SRX command without a locked DLL during self refresh abort	tXS_ABORT(min)	tRFC4(min)+10ns	–	tRFC4(min)+10ns	–	tRFC4(min)+10ns	–	nCK	
Exit self refresh to ZQCL, ZQCS, and MRS (CL, CWL, WR, RTP, and gear down)	tXS_FAST(min)	tRFC4(min)+10ns	–	tRFC4(min)+10ns	–	tRFC4(min)+10ns	–	nCK	
Exit self refresh for commands requiring a locked DLL	tXSDLL	tDLLK(min)	–	tDLLK(min)	–	tDLLK(min)	–	nCK	
Minimum CKE low width from self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	–	tCKE(min)+1nCK	–	tCKE(min)+1nCK	–	nCK	
Minimum CKE low width for self refresh entry/exit timing	tCKESR_PAR	tCKE(min)+1n	–	tCKE(min)+	–	tCKE(min)+1n	–	nCK	

with CA parity enabled		CK+PL		1nCK+PL		CK+PL			
Valid clock requirement after SRE (Self Refresh Entry) or PDE (Power-Down Entry)	tCKSRE	max(5nCK, 10ns)	–	max(5nCK, 10ns)	–	max(5nCK, 10ns)	–	nCK	
Valid clock requirement after SRE (Self Refresh Entry) or Power-Down with CA parity enabled	tCKSRE_PAR	Max(5nCK, 10ns)+PL	–	Max(5nCK, 10ns)+PL	–	max(5nCK, 10ns)+PL	–	nCK	
Valid clock requirement before SRX (Self Refresh Exit), PDX (Power-Down Exit), or Reset Exit	tCKSRX	max(5nCK, 10ns)	–	max(5nCK, 10ns)	–	max(5nCK, 10ns)	–	nCK	
Exit Power-Down from any valid command (DLL locked); Exit Precharge Power-Down (DLL frozen, no locked DLL required)	tXP	max(4nCK, 6ns)	–	max(4nCK, 6ns)	–	max(4nCK, 6ns)	–	nCK	
Minimum CKE pulse width	tCKE	max(3nCK, 5ns)	–	max(3nCK, 5ns)	–	max(3nCK, 5ns)	–	nCK	31, 32
Command Pass Disable Delay	tCPDED	4	–	4	–	4	–	nCK	
Power-Down Entry and Exit Time	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK	6
ACT Command to Power-Down Entry Time	tACTPDEN	1	–	1	–	2	–	nCK	7
PRE or PREA Command to Power-Down Entry Time	tPRPDEN	1	–	1	–	2	–	nCK	7
RD/RDA Command to Power-Down Entry Time	tRDPDEN	RL+4+1	–	RL+4+1	–	RL+4+1	–	nCK	
WR Command to Power-Down Timing (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	–	WL+4+(tWR/tCK(avg))	–	WL+4+(tWR/tCK(avg))	–	nCK	4
WRA Command Power-Down Timing (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	–	WL+4+WR+1	–	WL+4+WR+1	–	nCK	5
WR Command Power-Down Timing (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/tCK(avg))	–	WL+2+(tWR/tCK(avg))	–	WL+2+(tWR/tCK(a	–	nCK	4

						vg))			
WRA Command Power-Down Timing (BC4MRS)	tWRAPBC4DEN	WL+2+WR+1	–	WL+2+WR+1	–	WL+2+WR+1	–	nCK	5
REF Command to Power-Down Entry Time	tREFPDEN	1	–	1	–	2	–	nCK	7
MRS Command to Power-Down Entry Time	tMRSPDEN	tMOD(min)	–	tMOD(min)	–	tMOD(min)	–	nCK	
Mode Register Set Command Cycle Time in PDA Mode	tMRD_PDA	max(16nCK,10ns)	–	max(16nCK,10ns)	–	max(16nCK,10ns)	–	nCK	
Mode Register Set command update delay time in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		nCK	
Asynchronous RTT turn-on delay (DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change deviation	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	

Table 74 continued

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
First program the rising edge of DQS_t/DQS_n after write leveling mode	tWLMRD	40	–	40	–	40	–	nCK	12
DQS_t/DQS_n delay after write leveling mode	tWLDQSEN	25	–	25	–	25	–	nCK	12
Write Leveling Setup Time from rising CK_t/CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	–	0.13	–	0.13	–	tCK(avg)	
Write leveling hold time: from DQS_t/DQS_n crossing to CK_t/CK_c crossing	tWLH	0.13	–	0.13	–	0.13	–	tCK(avg)	
Write Leveling Output Delay	tWLO	0	9.5	0	9.5	0	9.5	ns	

Write Leveling Output Error	tWLOE	0	2	0	2	0	2	ns	
Commands not guaranteed to be executed during this period	tPAR_UNKNOWN	–	PL	–	PL	–	PL	nCK	
Delay from erroneous command to ALERT_n assertion	tPAR_ALERT_ON	–	PL+6nCK	–	PL+6ns	–	PL+6ns	nCK	
ALERT_n pulse width when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	nCK	
Time from Alert assertion to when controller must begin providing DES commands in persistent CA parity mode	tPAR_ALERT_RSP	–	43	–	50	–	57	nCK	
Parity latency	PL			4				nCK	
CRC error to ALERT_n delay	tCRC_ALERT	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	nCK	
Exit Reset from CKE high to valid MRS command (T2/Reset)	tXPR_GEAR	tXPR						nCK	
CKE high assertion to gear-down enable time (T2/CKE)	tXS_GEAR	tXS						nCK	
MRS command sync pulse time (T3)	tSYNC_GEAR	tMOD+4CK						nCK	27
Sync pulse to first valid command (T4)	tCMD_GEAR	tMOD						nCK	27
Gear-down setup time	tGEAR_setup	–	–	2	–	2	–	nCK	
Gear-down hold time	tGEAR_hold	–	–	2	–	2	–	nCK	
tRFC1 (min)	2Gb	160	–	160	–	160	–	ns	34
	4Gb	260	–	260	–	260	–	ns	34
	8Gb	350	–	350	–	350	–	ns	34
	16Gb	550	–	550	–	550	–	ns	34
tRFC2 (min)	2Gb	110	–	110	–	110	–	ns	34
	4Gb	160	–	160	–	160	–	ns	34
	8Gb	260	–	260	–	260	–	ns	34

	16Gb	350	–	350	–	350	–	ns	34
tRFC3 (min)	2Gb	90	–	90	–	90	–	ns	34
	4Gb	110	–	110	–	110	–	ns	34
	8Gb	160	–	160	–	160	–	ns	34
	16Gb	260	–	260	–	260	–	ns	34

Table 75: DDR4-2666 to DDR4-3200 Speed Grade Timing Parameters

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Minimum Clock Cycle Time (DLL Off Mode)	tCK(DLL_OFF)	8	20	8	20	8	20	8	20	ns	–
Average Clock Period	tCK(avg)	0.833	<0.937	0.75	<0.833	0.682	<0.75	0.625	<0.682	ns	35, 36
Average High Pulse Width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average Low Pulse Width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	Min = tCK(avg)min + tJIT(per)min_tot Max = tCK(avg)max + tJIT(per)max_tot								tCK(avg)	
Absolute Clock High Pulse Width	tCH(abs)	0.45	–	0.45	–	0.45	–	0.45	–	tCK(avg)	23
Absolute Clock Low Pulse Width	tCL(abs)	0.45	–	0.45	–	0.45	–	0.45	–	tCK(avg)	24
Clock Period Jitter - Total	JIT(per)_tot	-42	42	-38	38	-34	34	-32	32	ps	23
Clock Period Jitter - Deterministic	JIT(per)_dj	-21	21	-19	19	-17	17	-16	16	ps	26
Clock Period Jitter during DLL Locking	tJIT(per, lck)	-33	33	-30	30	-27	27	-25	25	ps	
Cycle to Cycle Jitter	tJIT(cc)	–	83	–	75	–	68	–	62	ps	
Cycle to Cycle Jitter during DLL Locking	tJIT(cc, lck)	–	67	–	60	–	55	–	50	ps	
Cumulative Error across 2	tERR(2pe	-61	61	-5	55	-50	50	-46	46	ps	

Cycles	r)			5							
Cumulative error across 3 cycles	tERR(3per)	-73	73	-66	66	-60	60	-55	55	ps	
Cumulative error across 4 cycles	tERR(4per)	-81	81	-73	73	-66	66	-61	61	ps	
Cumulative error across 5 cycles	tERR(5per)	-87	87	-78	78	-71	71	-65	65	ps	
Cumulative error across 6 cycles	tERR(6per)	-92	92	-83	83	-75	75	-69	69	ps	
Cumulative error across 7 cycles	tERR(7per)	-97	97	-87	87	-79	79	-73	73	ps	
Cumulative error across 8 cycles	tERR(8per)	-101	101	-91	91	-83	83	-76	76	ps	
Cumulative error across 9 cycles	tERR(9per)	-104	104	-94	94	-85	85	-78	78	ps	
Cumulative error across 10 cycles	tERR(10per)	-107	107	-96	96	-88	88	-80	80	ps	
Cumulative error across 11 cycles	tERR(11per)	-110	110	-99	99	-90	90	-83	83	ps	
Cumulative error across 12 cycles	tERR(12per)	-112	112	-101	101	-92	92	-84	84	ps	
Cumulative error across 13 cycles	tERR(13per)	-114	114	-103	103	-93	93	-86	86	ps	
Cumulative error across 14 cycles	tERR(14per)	-116	116	-104	104	-95	95	-87	87	ps	
Cumulative error across 15 periods	tERR(15per)	-118	118	-106	106	-97	97	-89	89	ps	
Cumulative error across 16 periods	tERR(16per)	-120	120	-108	108	-98	98	-90	90	ps	
Cumulative error across 17 periods	tERR(17per)	-122	122	-110	110	-100	100	-92	92	ps	
Cumulative error across 18 periods	tERR(18per)	-124	124	-112	112	-101	101	-93	93	ps	
Cumulative error across n = 13, 14 ... 49, 50 periods	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)								ps	

Command and Address Setup Time to CK_t, CK_c Refer to Vih(ac) / Vil(ac) standard	tIS(base)	62	-	55	-	48	-	40	-	ps	
Command and Address Setup Time to CK_t, CK_c Refer to Vref standard	tIS(Vref)	162	-	145	-	138	-	130	-	ps	
Command and Address Hold Time to CK_t, CK_c Refer to Vih(dc) / Vil(dc) standard	tIH(base)	87	-	80	-	73	-	65	-	ps	
Command and Address Hold Time to CK_t, CK_c Reference to Vref standard	tIH(Vref)	162	-	145	-	138	-	130	-	ps	

Table 75 (continued)

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Control and Address Input Pulse	tIPW	410	-	385	-	365	-	340	-	ps	
CAS_n to CAS_n Command Delay for Same Bank Group	tCCD_L	Max(5nCK, 5 ns)	-	Max(5nCK, 5 ns)	-	Max(5nCK, 5ns)	-	Max(5nCK, 5 ns)	-	nCK	34
CAS_n to CAS_n Command Delay for Different Bank Groups	tCCD_S	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command Delay for Different Bank Groups (2KB Page Size)	tRRD_S(2K)	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	34

ACTIVATE to ACTIVATE Command Delay for Different Bank Groups (1KB Page Size)	tRRD_S(1K)	Max(4nCK, 3.3ns)	–	Max(4nCK, 3ns)	–	Max(4nCK, 2.7ns)	–	Max(4nCK, 2.5ns)	–	nCK	34
Activate to activate command delay for different bank groups (1/2KB page size)	tRRD_S(1/2K)	Max(4nCK, 3.3ns)	–	Max(4nCK, 3ns)	–	Max(4nCK, 2.7ns)	–	Max(4nCK, 2.5ns)	–	nCK	34
Activate to activate command delay for the same bank group (2KB page size)	tRRD_L(2K)	Max(4nCK, 6.4ns)	–	Max(4nCK, 6.4ns)	–	Max(4nCK, 6.4ns)	–	Max(4nCK, 6.4ns)	–	nCK	34
Activate to activate command delay for the same bank group (1KB page size)	tRRD_L(1K)	Max(4nCK, 4.9ns)	–	Max(4nCK, 4.9ns)	–	Max(4nCK, 4.9ns)	–	Max(4nCK, 4.9ns)	–	nCK	34
ACTIVATE to ACTIVATE Command Delay for Same Bank Group (1KB Page Size)	tRRD_L(1/2K)	Max(4nCK, 4.9ns)	–	Max(4nCK, 4.9ns)	–	Max(4nCK, 4.9ns)	–	Max(4nCK, 4.9ns)	–	nCK	34
Four activate windows (2KB page size)	tFAW_2K	Max(28nCK, 30ns) 30ns)	–	Max(28nCK, 30ns) 30ns)	–	Max(28nCK, 30ns)	–	Max(28nCK, 30ns)	–	ns	34
Four activate windows (1KB page size)	tFAW_1K	Max(20nCK, 21ns) 21ns)	–	Max(20nCK, 21ns) 21ns)	–	Max(20nCK, 21ns)	–	Max(20nCK, 21ns)	–	ns	34
Four activate windows (1/2KB page size)	tFAW_1/2K	Max(16nCK, 13ns)	–	Max(16nCK, 12ns)	–	Max(16nCK, 10.875ns)	–	Max(16nCK, 10ns)	–	ns	34
Internal write transaction to internal read command delay for different bank groups	tWTR_S	max(2nCK	–	max(2nCK	–	Max(2nCK	–	Max(2nCK	–	ns	1, 2,

		, 2.5ns)		, 2.5ns)		, 2.5ns)		, 2.5ns)			34
Internal write transaction to internal read command delay for the same bank group	tWTR_L	Max(4nCK, 7.5ns)	–	Max(4nCK, 7.5ns)	–	Max(4nCK, 7.5ns)	–	Max(4nCK, 7.5ns)	–	ns	1, 34
Internal read command to precharge command delay	tRTP	Max(4nCK, 7.5ns)	–	Max(4nCK, 7.5ns)	–	Max(4nCK, 7.5ns)	–	Max(4nCK, 7.5ns)	–	ns	34
Write recovery time	tWR	15	–	15	–	15	–	15	–	ns	1
Write recovery time with CRC and DM enabled	tWR_CRC_DM	tWR+max(4nCK, 3.75ns)	–	tWR+max(4nCK, 3.75ns)	–	tWR+max(5nCK, 3.75ns)	–	tWR+max(5nCK, 3.75ns)	–	ns	1, 28
Write to read command delay for different bank groups with CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max(4nCK, 3.75ns)	–	tWTR_S+max(4nCK, 3.75ns)	–	tWTR_S+max(5nCK, 3.75ns)	–	tWTR_S+max(5nCK, 3.75ns)	–	ns	2, 29, 34
Write to read command delay for same bank group with CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max(4nCK, 3.75ns)	–	tWTR_L+max(4nCK, 3.75ns)	–	tWTR_L+max(5nCK, 3.75ns)	–	tWTR_L+max(5nCK, 3.75ns)	–	ns	3, 30, 34
DLL locking time	tDLLK	768	–	854	–	940	–	1024	–	nCK	
Mode Register Set command cycle time	tMRD	8	–	8	–	8	–	8	–	nCK	
Mode Register Set command update delay	tMOD	Max(24nCK, 15ns)	–	Max(24nCK, 15ns)	–	Max(24nCK, 15ns)	–	Max(24nCK, 15ns)	–	nCK	50
Multi-Purpose Register recovery time	tMPRR	1	–	1	–	1	–	1	–	nCK	33
Multi-Purpose Register write recovery time	tWR_MPR	tMOD(min)+AL + PL	–	tMOD(min)+AL + PL	–	tMOD(min)+AL + PL	–	tMOD(min)+AL + PL	–	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))								nCK	
DQ0 or DQ0 driven to 0 setup time to first DQS rising edge	tPDA_S	0.5	–	0.5	–	0.5	–	0.5	–	UI	45, 47

DQ0 or DQ0 driven to 0 hold time from last DQS falling edge	tPDA_H	0.5	–	0.5	–	0.5	–	0.5	–	UI	46, 47
CS_n to command address delay	tCAL	Max (3 nCK, 3.748 ns)	–	Max (3 nCK, 3.748 ns)	–	Max (3 nCK, 3.748 ns)	--	Max (3 nCK, 3.748 ns)	–	nCK	
Mode Register Set command cycle time in CAL mode	tMRD_tCAL	tMOD+tCAL	–	tMOD+tCAL	–	tMOD+tCAL	–	tMOD+tCAL	–	nCK	
Update delay in CAL mode of mode register setting	tMOD_tCAL	tMOD+tCAL	–	tMOD+tCAL	–	tMOD+tCAL	–	tMOD+tCAL	–	nCK	

Table 75 (continued)

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Per group, per access: DQS_t, DQS_c to DQ slew rate	tDQSQ	–	0.17	–	0.18	–	–	–	–	tCK(avg)/2	13, 18, 39, 49
Per access DQS_t, DQS_c, per group DQ output hold time	tQH	0.74	–	0.74	–	–	–	–	–	tCK(avg)/2	13, 17, 18, 39, 49
Data valid window per device per UI: (tQH – tDQSQ) per UI on a given DRAM	tDVWd	0.64	–	TBD	–	–	–	–	–	UI	17, 18, 39, 49
Data valid window per pin per UI: (tQH – tDQSQ) per UI on a given pin of a DRAM	tDVWp	0.72	–	0.72	–	–	–	0.72	–	UI	17, 18, 39, 49
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-330	175	-310	170	-280	165	-250	160	ps	39
DQ high-impedance time from CK_t, CK_c	tHZ(DQ)	–	175	–	170	–	165	–	160	ps	39
DQS_t, DQS_c differential read preamble (1-clock preamble)	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	tCK	39, 40
DQS_t, DQS_c differential read preamble (2-clock preamble)	tRPRE2	1.8	NOTE44	1.8	NOTE44	1.8	NOTE44	1.8	NOTE44	tCK	39, 41
DQS_t, DQS_c differential read postamble	tRPST	0.33	NOTE45	0.33	NOTE45	0.33	NOTE45	0.33	NOTE45	tCK	39
DQS_t, DQS_c differential output high time	tQSH	0.4	–	0.4	–	0.4	–	0.4	–	tCK	21, 39
DQS_t, DQS_c differential output low time	tQSL	0.4	–	0.4	–	0.4	–	0.4	–	tCK	20, 39
DQS_t, DQS_c differential write preamble (1-clock	tWPRE	0.9	–	0.9	–	0.9	–	0.9	–	tCK	42

preamble)											
DQS_t, DQS_c differential write preamble (2-clock preamble)	tWPRE2	1.8	–	1.8	–	1.8	–	1.8	–	tCK	43
DQS_t, DQS_c differential write postamble	tWPST	0.33	–	0.33	–	0.33	–	0.33	–	tCK	
DQS_t and DQS_c low-impedance time (refer to RL-1)	tLZ(DQS)	-330	175	-310	170	-280	165	-250	160	ps	39
DQS_t and DQS_c high-impedance time (refer to RL+BL/2)	tHZ(DQS)	–	175	–	170	–	165	–	160	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c Differential Input High Pulse Width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c Rising Edge to CK_t, CK_c Rising Edge (1 Clock Preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c Rising Edge to CK_t, CK_c Rising Edge (2 Clock Preamble)	tDQSS2	_	_	_	_	–	–	–	–	tCK	43
DQS_t, DQS_c Falling Edge Setup Time to CK_t, CK_c Rising Edge	tDSS	0.18	–	0.18	–	0.18	–	0.18	–	tCK	
DQS_t, DQS_c Falling Edge Hold Time to CK_t, CK_c Rising Edge	tDSH	0.18	–	0.18	–	0.18	–	0.18	–	tCK	
DQS_t, DQS_c Rising Edge Output Timing Position from Rising CK_t, CK_c with DLL Enabled Mode	tDQSCK (DLL On)	-175	175	-170	170	-165	165	-160	160	ps	37, 38, 39
DQS_t, DQS_c per DRAM Rising Edge Output Variance Window	tDQSCKI (DLL On)		290		270		265		260	ps	37, 38, 39
Command Path Disable MPSM Entry Delay	tMPED	Min = tMOD(min) + tCPDED(min)								nCK	
Valid Clock Requirement After MPSM	tCKMPE	Min = tMOD(min) +								nCK	

Entry		tCPDED(min)									
Valid Clock Requirement Before MPSM Exit	tCKMPX	Min = tCKSRX (min)								nCK	
MPSM Exit to Command Not Requiring DLL Lock	tXMP	tXS(min)								nCK	
MPSM Exit to Command Requiring DLL Lock	tXMPDLL	Min = tXMP(min) + tXSDLL(min)								nCK	
CS_n setup time to CKE	tMPX_S	Min = tIS(min) + tIH(min)								ns	
CS_n high hold time to CKE rising edge	tMPX_HH	Min = tXP								ns	
CS_n low hold time to CKE rising edge	tMPX_IH	Min = 12; Max = tXMP-10ns								ns	
Power-up and reset calibration time	tZQinit	1024	–	1024	–	1024	–	1024	–	nCK	
Normal operation full calibration time	tZQoper	512	–	512	–	512	–	512	–	nCK	
Normal operation short calibration time	tZQCS	128	–	128	–	128	–	128	–	nCK	

Table 75 (continued)

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
From CKE high to a valid command (Reset Exit)	tXPR	Max(5nCK, tRFC(min)+10ns)	–	max(5nCK, tRFC(min)+10ns)+10ns)	–	max(5nCK, tRFC(min)+10ns)	–	max(5nCK, tRFC(min)+10ns)	–	nCK	
Exit self refresh for commands not requiring a locked DLL	tXS	tRFC(min)+10ns 10ns	–	tRFC(min)+ 10ns	–	tRFC(min)+ 10ns	–	tRFC(min)+ 10ns	–	nCK	
SRX command without a locked DLL during self refresh abort	tXS_ABORT(min)	tRFC4(min)+ 10ns	–	tRFC4(min)+ 10ns	–	tRFC4(min)+ 10ns	–	tRFC4(min)+10ns	–	nCK	
Exit self refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP, and gear down)	tXS_FAST (min)	tRFC4(min)+ 10ns	–	tRFC4(min)+ 10ns	–	tRFC4(min)+ 10ns	–	tRFC4(min)+10ns	–	nCK	

Exit self refresh for commands requiring a locked DLL	tXSDLL	tDLLK(min)	–	tDLLK(min)	–	tDLLK(min)	–	tDLLK(min)	–	nCK	
Minimum CKE low width from self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	–	tCKE(min)+1nCK	–	tCKE(min)+1nCK	–	tCKE(min)+1nCK	–	nCK	
Minimum CKE low width for self refresh entry/exit timing with CA parity enabled	tCKESR_PAR	tCKE(min)+1nCK+PL	–	tCKE(min)+1nCK+PL	–	tCKE(min)+1nCK+PL	–	tCKE(min)+1nC K+PL	–	nCK	
Valid clock requirement after SRE (Self Refresh Entry) or PDE (Power-Down Entry)	tCKSRE	max(5nCK,10ns)	–	max(5nCK,10ns)	–	max(5nCK,10ns)	–	max(5nCK,10ns)	–	nCK	
Valid clock requirement after SRE (Self Refresh Entry) or Power-Down with CA parity enabled	tCKSRE_PAR	Max(5nCK,10ns)+PL	–	Max(5nCK,10ns)+PL	–	max(5nCK,10ns)+PL	–	max(5nCK,10ns)+PL	–	nCK	
Valid clock requirement before SRX (Self Refresh Exit), PDX (Power-Down Exit), or Reset Exit	tCKSRX	max(5nCK,10ns)	–	max(5nCK,10ns)	–	max(5nCK,10ns)	–	max(5nCK,10ns)	–	nCK	
Exit power-down with DLL for any valid command; exit precharge power-down with DLL frozen for commands not requiring a locked DLL	tXP	max(4nCK,6ns)	–	max(4nCK,6ns)	–	max(4nCK,6ns)	–	max(4nCK,6ns)	–	nCK	
Minimum CKE pulse width	tCKE	max(3nCK,5ns)	–	max(3nCK,5ns)	–	max(3nCK,5ns)	–	max(3nCK,5ns)	–	nCK	31, 32
Command Pass Disable Delay	tCPDED	4	–	4	–	4	–	4	–	nCK	
Power-Down Entry and Exit Time	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK	6
ACT Command to Power-Down Entry Time	tACTPDEN	2	–	2	–	2	–	2	–	nCK	7
PRE or PREA Command to Power-Down Entry Time	tPRPDEN	2	–	2	–	2	–	2	–	nCK	7

RD/RDA Command to Power-Down Entry Time	tRDPDEN	RL+4+1	–	RL+4+1	–	RL+4+1	–	RL+4+1	–	nCK	
WR Command to Power-Down Timing (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	–	WL+4+(tWR/tCK(avg))	–	WL+4+(tWR/tCK(avg))	–	WL+4+(tWR/tCK(avg))	–	nCK	4
WRA Command Power-Down Timing (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	–	WL+4+WR+1	–	WL+4+WR+1	–	WL+4+WR+1	–	nCK	5
WR Command Power-Down Timing (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/tCK(avg))	–	WL+2+(tWR/tCK(avg))	–	WL+2+(tWR/tCK(avg))	–	WL+2+(tWR/tCK(avg))	–	nCK	4
WRA Command Power-Down Timing (BC4MRS)	tWRAPBC4DEN	WL+2+WR+1	–	WL+2+WR+1	–	WL+2+WR+1	–	WL+2+WR+1	–	nCK	5
REF Command to Power-Down Entry Time	tREFPDEN	2	–	2	–	2	–	2	–	nCK	7
MRS Command to Power-Down Entry Time	tMRSPDEN	tMOD(min)	–	tMOD(min)	–	tMOD(min)	–	tMOD(min)	–	nCK	
Mode Register Set Command Cycle Time in PDA Mode	tMRD_PDA	max(16nCK, 10ns)	–	max(16nCK, 10ns)	–	max(16nCK, 10ns)	–	max(16nCK, 10ns)	–	nCK	
Mode Register Set command update delay time in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		nCK	
Asynchronous RTT turn-on delay (DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change deviation	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	

Table 75 (continued)

Speed		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
First program the rising edge of DQS_t/DQS_n after write leveling mode	tWLMRD	40	–	40	–	40	–	40	–	nCK	12
DQS_t/DQS_n delay after write leveling mode	tWLDQSEN	25	–	25	–	25	–	25	–	nCK	12
Write Leveling Setup Time from rising CK_t/CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	–	0.13	–	0.13	–	0.13	–	tCK(avg)	
Write Leveling Hold Time from rising DQS_t/DQS_n crossing to rising CK_t/CK_c crossing	tWLH	0.13	–	0.13	–	0.1	–	0.13	–	tCK(a	

						3				vg)	
Write Leveling Output Delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write Leveling Output Error	tWLOE	0	2	0	2	0	2	0	2	ns	
Commands not guaranteed to be executed during this period	tPAR_UNKNOWN	–	PL	–	PL	–	PL	–	PL	nCK	
Delay from erroneous command to ALERT_n assertion	tPAR_ALERT_ON	–	PL+6ns	–	PL+6ns	–	PL+6ns	–	PL+6ns	nCK	
ALERT_n pulse width when asserted	tPAR_ALERT_PW	72	144	80	160	88	176	96	192	nCK	
Time from Alert assertion to when controller must begin providing DES commands in persistent CA parity mode	tPAR_ALERT_RSP	–	64	–	71	–	78	–	85	nCK	
Parity latency	PL	5		5		6		6		nCK	
CRC error to ALERT_n delay	tCRC_ALERT	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	nCK	
Exit Reset from CKE high to valid MRS command (T2/Reset)	tXPR_GEAR	–	–	tXPR						nCK	
CKE high assertion to gear-down enable time (T2/CKE)	tXS_GEAR	–	–	tXS						nCK	
MRS command sync pulse time (T3)	tSYNC_GEAR	–	–	tMOD+4 CK						nCK	27
Sync pulse to first valid command (T4)	tCMD_GEAR	–	–	tMOD						nCK	27
Gear-down setup time	tGEAR_setup	–	–	2	–	2	–	2	–	nCK	
Gear-down hold time	tGEAR_hold	–	–	2	–	2	–	2	–	nCK	
tRFC1 (min)	2Gb	160	–	160	–	160	–	160	–	ns	34
	4Gb	260	–	260	–	260	–	260	–	ns	34
	8Gb	350	–	350	–	350	–	350	–	ns	34
	16Gb	550	–	550	–	550	–	550	–	ns	34
tRFC2 (min)	2Gb	110	–	110	–	110	–	110	–	ns	34
	4Gb	160	–	160	–	160	–	160	–	ns	34
	8Gb	260	–	260	–	260	–	260	–	ns	34
	16Gb	350	–	350	–	350	–	350	–	ns	34
tRFC4 (min)	2Gb	90	–	90	–	90	–	90	–	ns	34

4Gb	110	–	110	–	110	–	110	–	ns	34
8Gb	160	–	160	–	160	–	160	–	ns	34
16Gb	260	–	260	–	260	–	260	–	ns	34

Note:

1. The start of an internal write transaction is defined as follows:
   For BL8 (by MRS and on-the-fly): 4 clock cycles after the rising clock edge at WL. For BC4 (on-the-fly): 4 clock cycles after the rising clock edge at WL.
   For BC4 (MRS fixed): 2 clock cycles after the rising clock edge at WL.
2. When both CRC and DM are enabled, a separate timing parameter will cover the write-to-read delay.
3. Commands requiring DLL lock are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns; to calculate tWRPDEN, tWR/tCK should be rounded according to the rounding algorithm defined in section 14.5.
5. WR (Write Recovery) in clock cycles is programmed via MR0.
6. tREFI depends on T_OPER.
7. When operations such as row activation, precharge, auto refresh, or refresh are in progress, CKE may be registered LOW; however, the power-down IDD specification will not apply until these operations are completed.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK] = RU{tPARAM[ns] / tCK(avg)[ns]}, expressed in clock cycles, assuming all input clock jitter specifications are met.
9. When both CRC and DM are enabled, use tWR_CRC_DM instead of tWR.
10. When both CRC and DM are enabled, tWTR_S_CRC_DM is used instead of tWTR_S.
11. When both CRC and DM are enabled, tWTR_L_CRC_DM is used instead of tWTR_L.
12. The maximum value depends on the system.
13. Total time per group from DQ to DQS, where the total time includes the sum of deterministic and random time components for a specified bit error rate. The bit error rate specification and measurement method are to be determined.
14. Deterministic component of total timing. Measurement method to be determined.
15. Static offset per group from DQ to DQS. Measurement method to be determined.
16. This parameter will be characterized and guaranteed in design.
17. When the device operates with input clock jitter, this parameter must be derated according to the actual tjit(per)_total of the input clock. (Output derating relative to the SDRAM input clock). Example TBD.
18. Disable DRAM DBI mode.
19. Enable DRAM DBI mode. Supported only on x8 and x16 DRAMs.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, measured from a falling edge to the next consecutive rising edge.
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, measured from a rising edge to the next falling edge.
22. There is no maximum cycle time limit other than meeting the refresh interval tREFI.
23. tCH(abs) is the absolute instantaneous clock high pulse width, measured from a rising edge to the next falling edge.
24. tCL(abs) is the absolute instantaneous clock low pulse width, measured from a falling edge to the next rising edge.
25. Total jitter includes the sum of deterministic jitter and random jitter components for a specified BER. The BER target and measurement method are given.

26. The deterministic jitter component is extracted from total jitter. This parameter is determined by design and guaranteed.
27. This parameter must be an even number of clocks.
28. When both CRC and DM are enabled, use tWR_CRC_DM instead of tWR.
29. When both CRC and DM are enabled, use tWTR_S_CRC_DM instead of tWTR_S.
30. When both CRC and DM are enabled, use tWTR_L_CRC_DM instead of tWTR_L.
31. After CKE is registered LOW, the CKE signal level shall be maintained below VILDC for the tCKE specification (low pulse width).
32. After CKE is registered HIGH, the CKE signal level shall be maintained above VIHDC for the tCKE specification (high pulse width).
33. Defined between the end of an MPR read burst and the MRS to reload MPR or disable MPR function.
34. Parameters from tCK(avg)min to tCK(avg)max apply to all standard JEDEC clock cycle values as described in the Speed Bin tables.
35. This parameter must be consistent with the Speed-Bin Tables shown in Option 11.
36. DDR4-1600 AC timing applies for DRAM operation at data rates below 1600 MT/s. UI = tCK(avg) min / 2
37. Applied when DRAM is in DLL ON mode.
38. Assumes no jitter on the clock signal input to the DRAM.
39. This value is valid only when RZQ/7 RONNOM = 34 ohm.
40. 1tCK switching mode, set MR4:A11 to 0.
41. 2tCK switching mode, set MR4:A11 to 1, applicable for DDR4-2400/2666/3200 speed grades.
42. 1tCK mode, set MR4:A12 to 0.
43. 2tCK mode, set MR4:A12 to 1, applicable for DDR4-2400/2666/3200 speed grades.
44. Maximum read preamble is bounded by tLZ(DQS) min on the left and tDQSCK(max) on the right.
45. Midpoint of DQ falling transition from high to low to first rising edge of DQS differential crosspoint.
46. DQS differential crosspoint to last falling edge of DQ rising signal midpoint.
47. The VrefDQ value must be set to its midpoint (Vcent_DQ) to capture either DQ0 high or low level to enter PDA mode.
48. Maximum read postamble is bounded by tDQSCK(min) + tQSH(min) on the left and tHZ(DQS) max on the right.
49. Specifies the reference level for DQ output signals, with the midpoint as the widest part of the output signal eye. This midpoint should be approximately 0.7 * VDDQ, serving as the center level of the static single-ended output peak-to-peak swing, with driver impedance of 34 ohms and effective test load of 50 ohms to VTT = VDDQ.
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

14.5 Rounding Algorithm

Software algorithms for calculating timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33… MHz, or a clock period of 1.0714… ns. Similarly, a system with a memory clock frequency of 1066.66… MHz mathematically yields a clock period of 0.9375… ns. In most cases, it is impossible to accurately represent all digits after the decimal point, and rounding must be performed because the DDR4 SDRAM specification establishes a minimum granularity of 1 ps for timing parameters.

Rounding rules must be defined to optimize device performance without violating device parameters. These algorithms rely on results within the correction factor range of device testing and specifications to avoid performance loss due to rounding errors.

The rules are:

Clock period (e.g., tCKAVGmin) is defined with 1 ps precision; e.g., 0.9375… ns is defined as 937 ps and 1.0714… ns is defined as 1071 ps.

Using true math, parameters programmed in clock count (nCK) system, such as tAAmin, tRCDmin, etc., but expressed in

time units (ns), are divided by the clock period (ns), producing a unitless ratio, subtract a 2.5% correction factor, then set the result to the next higher clock integer.

nCK = ceiling [(parameter_in_ns / application_tCK_in_ns) - 0.025]

Alternatively, the programmer may prefer using integer math instead of true math, by expressing timings in ps, scaling the desired parameter value by 1000, dividing by the application clock period, adding a 97.4% inverse correction factor, dividing the result by 1000, then truncating to the next lower integer value:

nCK = truncate [{(parameter_in_ps x 1000) / (application_tCK_in_ps) + 974} / 1000]

Both algorithms produce the same result.

14.6 DQ Input Receiver Compliance Mask Voltage and Timing

The voltage and timing DQ input receiver compliance mask is shown in the figure below. The receiver mask (Rx mask) defines the region that the input signal must not encroach upon, in order for the DRAM input receiver to be expected to successfully capture a valid input signal with bit error rate of 1e-16; any input signal that intrudes into the Rx mask will be considered invalid data. The Rx mask is a receiver attribute per DQ input pin, not an effective data eye.

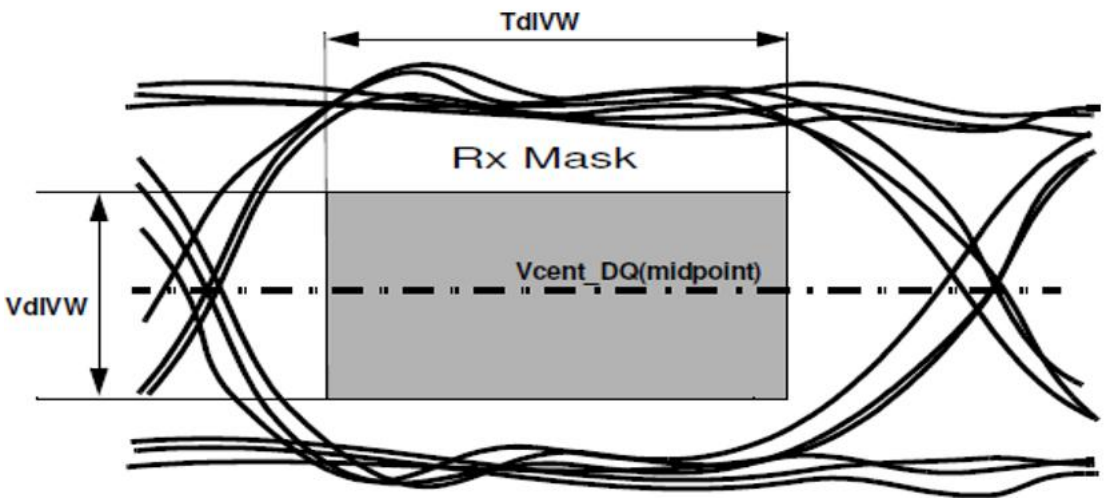


Figure 27 DQ Receiver (RX) Mask

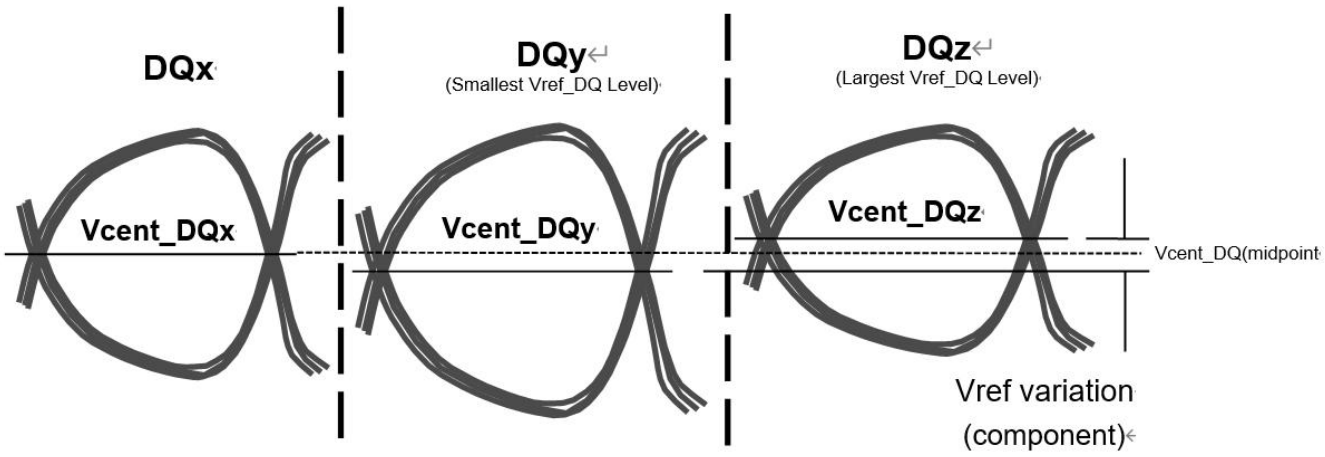
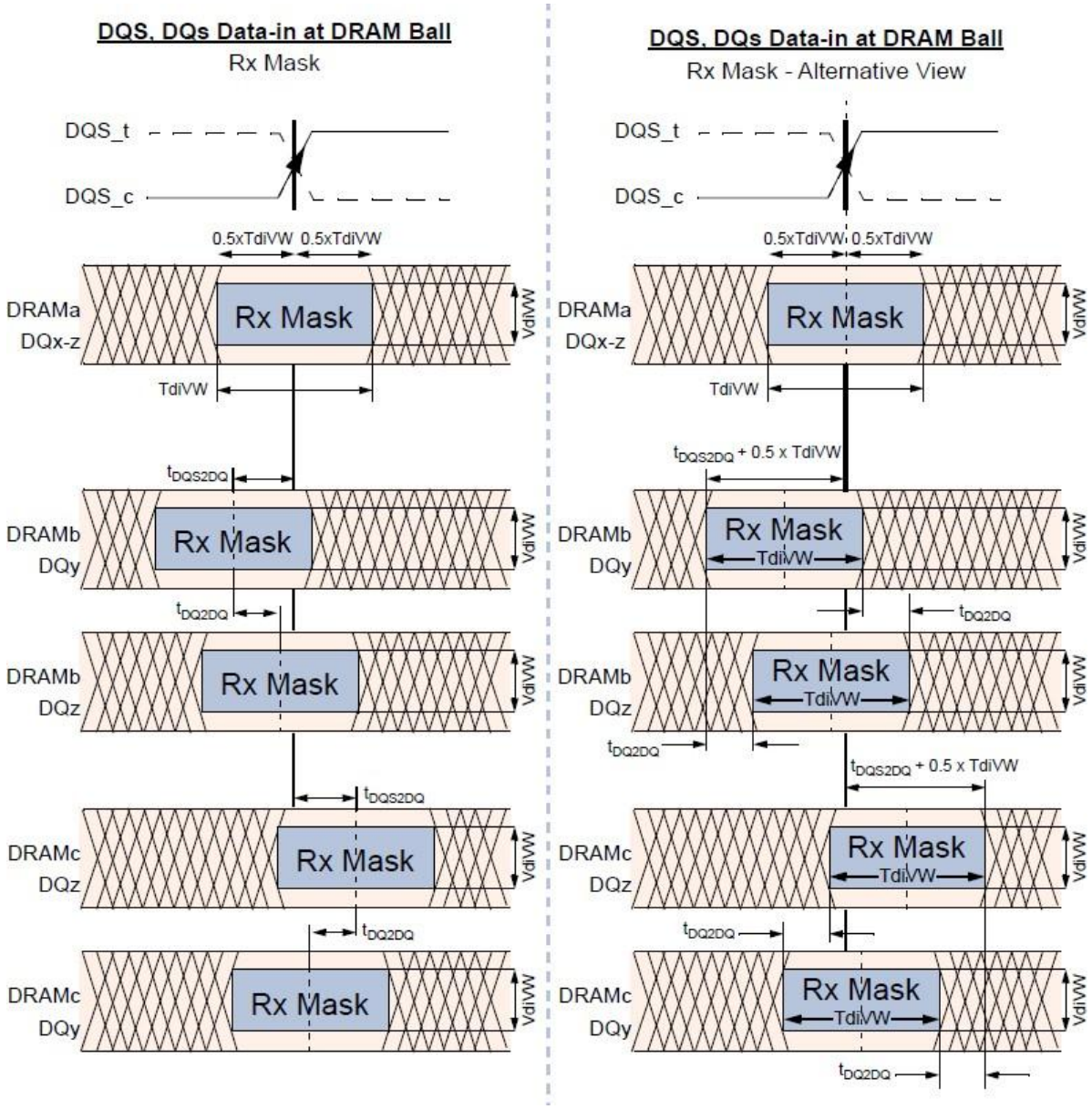


Figure 28 Vcent_DQ to Vcent_DQ Variation (Midpoint)

Vref_DQ voltage is an internal reference voltage level that must be set to the appropriate training setting, typically Vcent_DQ (midpoint), in order to obtain a valid Rx Mask value.

Vcent_DQ is defined as the midpoint between the maximum and minimum Vref_DQ voltage levels across all DQ pins of a

given DDR4 DRAM component, where each DQ pin's Vref level is defined by the center (i.e., widest opening) of the cumulative data input eye as shown in Figure 24. This clarifies that any DDR4 DRAM component-level variation must be accounted for within the DDR4 DRAM Rx mask. The component-level Vref will be set by the system to account for Ron and ODT settings.



Note:

DQx represents a best-centered mask. DRAMa represents a DRAM without DQS/DQ skew.

DQy represents the earliest valid mask. DRAMb represents a DRAM with early skew (negative tDQS2DQ).

DQz represents the latest valid mask. DRAMc represents a DRAM with delayed skew (positive tDQS2DQ).

Note:

1. The figure shows the allowable slopes between DRAM-to-DRAM and DQ-to-DQ.
2. The signals are assumed to be data-center aligned at the DRAM latch.
3. TdiPW is not shown; the composite data eye shown violates TdiPW.
4. VCENT_DQ (midpoint) is not shown but is assumed to be the midpoint of VdiVW.

Figure 29: DQS-to-DQ and DQ-to-DQ Timing for DRAM Pins

All timing items in Figure 29 are measured at the VdiVW level centered around Vcent_DQ (midpoint) and referenced to

the DQS_t/DQS_c center aligned with the DQ of each pin.

Rising edge slew rate is defined by srr1 and srr2. The measurement points for the rising edge slew rate are as shown in Figure 30: tr1 is measured from 0.5*VdiVW(max) below Vcent_DQ (midpoint) to the last 0.5*VdiVW(max) above Vcent_DQ (midpoint) for a low-to-high transition, and tr2 is measured from the last 0.5*VdiVW(max) above Vcent_DQ (midpoint) to the first 0.5*VIHL_AC(min) above Vcent_DQ (midpoint).

Rising Edge Slew Rate Equation:

srr1 = VdiVW(max) / tr1

srr2 = (VIHL_AC(min) - VdIVW(max)) / (2*tr2)

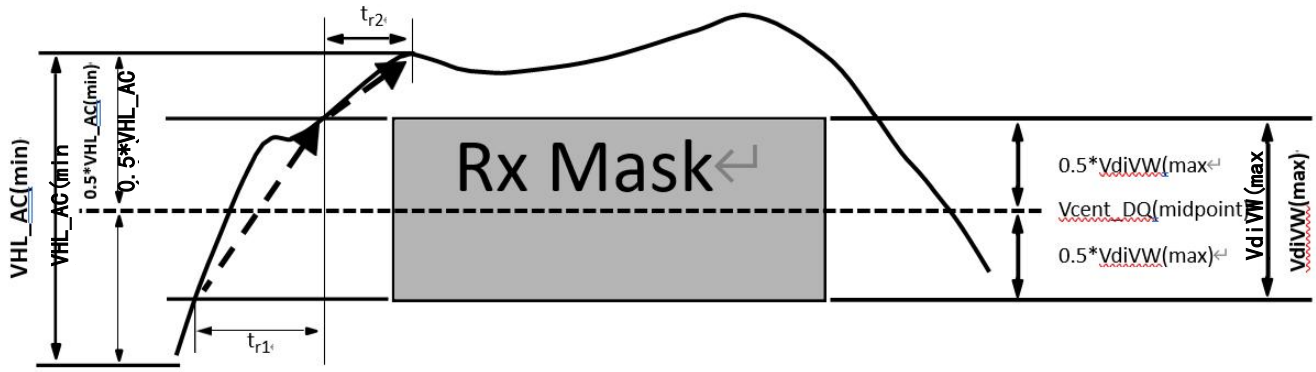


Figure 30 Rising Edge Slew Rate Condition

Falling edge slew rate is defined by srf1 and srf2. The measurement points for the falling edge slew rate are shown in Figure 31 below: measured from the last high-to-low transition tf1 from 0.5*VdiVW(max) above Vcent_DQ (midpoint) to 0.5*VdiVW(max) below Vcent_DQ (midpoint), and measured from the last 0.5*VdiVW(max) below Vcent_DQ (midpoint) to the first 0.5*VIHL_AC(min) below Vcent_DQ (pin midpoint) transition tf2.

Falling Edge Slew Rate Equation:

srf1 = VdiVW(max) / tf1

srf2 = (VIHL_AC(min) - VdIVW(max)) / (2*tf2)

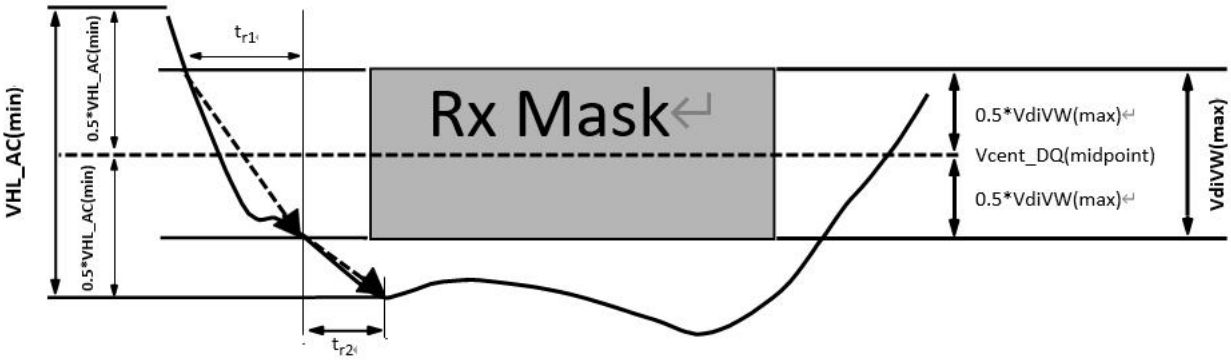


Figure 31 Falling Edge Slew Rate Condition

Table 80 DRAM DQ in Receive Mode; * UI = tCK(avg).min / 2

Symbol	Parameter	DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
VdIVW	RX Mask Voltage - pk-pk	-	130	-	120	-	115	-	110	mV	1,2,1

											0
TdIVW	Rx Timing Window	–	0.2	–	0.22	–	0.23	–	0.23	UI*	1,2,10
VIHL_AC	DQ AC input swing pk-pk	160	–	150	–	145	–	140	–	mV	3,4,10
TdIPW	DQ input pulse width	0.58	–	0.58	–	0.58	–	0.58	–	UI*	5,10
tDQS2DQ	Rx mask DQS to DQ skew	-0.17	0.17	-0.19	0.19	-0.22	0.22	-0.22	0.22	UI*	6, 10
tDQ2DQ	Rx mask DQ to DQ skew	–	tdb	–	0.105	–	0.115	–	0.125	UI*	7
srr1, srf1	If tCK >= 0.935ns, input slew rate exceeds VdIVW	1.0	9	1.0	tbd	1.0	tbd	tbd	tbd	V/ns	8,10
	If 0.935ns > tCK >= 0.625ns, input slew rate exceeds VdIVW	1.25	9	1.25	tbd	1.25	tbd	tbd	tbd	V/ns	8,10
srr2	Rising edge input slew rate, exceeding 1/2 VIHL_AC	0.2*srr1	9	0.2*srr1	tbd	0.2*srr1	tbd	tbd	tbd	V/ns	9,10
srf2	Falling edge input slew rate, exceeding 1/2 VIHL_AC	0.2*srf1	9	0.2*srf1	tbd	0.2*srf1	tbd	tbd	tbd	V/ns	9,10

Note:

1. After VrefDQ training is completed, VdIVW is the total input valid window of data Rx mask voltage and timing centered at Vcent_DQ (midpoint). The data Rx mask is applied on a per-bit basis and should include voltage and temperature drift terms. The input buffer design specification requires achieving at least BER = 1e-16 without violating the RxMask. If necessary, the dual Dirac method will be used to characterize and extrapolate BER from higher bit error rates (TBD).
2. Defined for DQ internal Vref range 1.

4. See overshoot and undershoot specifications.

5. The pulse signal swing at the DQ input to the receiver must meet or exceed VIHL(AC)(min). When both rising and falling edges occur within the same UI, i.e., valid tDIPW, VIHL(AC)(min) is achieved on a per-UI basis.

6. Minimum input pulse width defined at Vcent_DQ (midpoint).

7. DQS-to-DQ skew is the skew between DQS and DQ within a nibble (x4) or a byte (x8, x16) on the DDR4 SDRAM pins across process, voltage, and temperature.

8. DQ-to-DQ skew is the skew among DQ within a nibble (x4) or a byte (x8, x16) on the DDR4 SDRAM pins for a given component across process, voltage, and temperature.

9. Input slew rate on the VdIVW mask centered at Vcent_DQ (midpoint). The slowest and fastest DQ slew rates on each transition edge must be within 1.7 V/ns.

10. Input slew rate between the VdiVW mask edge and the VIH(AC)(min) and VIL(AC)(max) points.

11. All Rx mask specifications must be met for each UI. For example, if the minimum input pulse width is violated while meeting tDIVW(min), VdiVW(max), and the minimum slew rate limit, then tDIVW(min) or the minimum slew rate must be increased to the point where the minimum input pulse width is no longer violated.

14.7 Command, Control, and Address Setup, Hold, and Derating

The total required tIS (setup time) and tIH (hold time) are calculated by adding the datasheet tIS values, VIL(AC)/VIH(AC) points, and tIH values, VIL(DC)/VIH(DC) points, respectively, to the ΔtIS and ΔtIH derating values to account for slew rate variations. The base values are obtained at a single-ended signal slew rate of 1 V/ns and a differential clock slew rate of 2 V/ns. Example: tIS(total setup time) = tIS(base time) + ΔtIS. For a valid transition, the input signal must remain above/below VIH(AC)/VIL(AC) for the time defined by tVAC.

Although the total setup time for slow slew rates may be negative (e.g., at a rising clock transition, the valid input signal will not have reached VIH(AC)/VIL(AC)), a valid input signal is still required to complete the transition and reach VIH(AC)/VIL(AC). For slew rates falling between the values listed in the derating table, derating values can be obtained by linear interpolation.

The nominal slew rate for setup (tIS) of a rising signal is defined as the slew rate between the last crossing of VIL(DC)(max) and the first crossing of VIH(AC)(min), and this slew rate shall not be less than the specified minimum slew rate. The nominal slew rate for setup (tIS) of a falling signal is defined as the slew rate between the last crossing of VIH(DC)(min) and the first crossing of VIL(AC)(max), and this slew rate shall not be greater than the specified maximum slew rate.

The nominal slew rate for hold (tIH) of a rising signal is defined as the slew rate between the last crossing of VIL(DC)(max) and the first crossing of VIH(AC)(min), and this slew rate shall be not less than the specified minimum slew rate. The nominal slew rate for hold (tIH) of a falling signal is defined as the slew rate between the last crossing of VIH(DC)(min) and the first crossing of VIL(AC)(max), and this slew rate shall not exceed the specified maximum slew rate.

Table 81 – Command, Address, Control Setup and Hold Values

Symbol	2400	2666	2933	3200	Unit	Reference
tIS(base, AC100)	62	55	48	40	ps	VIH/L(ac)
tIH(base, DC75)	87	80	73	65	ps	VIH/L(dc)
tIS(base, AC tbd)	–	–	–	–	ps	VIH/L(ac)
tIH(base, DC tbd)	–	–	–	–	ps	VIH/L(dc)
tIS/tIH@VREF	162	145	138	130	ps	

Note:

1. Base AC/DC reference at 1 V/ns slew rate and 2 V/ns clock slew rate.
2. Values listed are for reference only; applicable limits are defined elsewhere.

Table 82 – Command, Address, Control Setup and Hold Values

Parameter	2400	2666	2933	3200	Unit	Reference
VIH.CA(AC)min	100	90	90	90	mV	VIH/L(ac)
VIH.CA(DC)min	75	65	65	65	mV	VIH/L(dc)
VIL.CA(AC)max	-75	-65	-65	-65	mV	VIH/L(ac)
VIL.CA(DC)max	-100	-90	-90	-90	mV	VIH/L(dc)

Note:

1. Command, address, control input levels referenced to VREFCA.
2. Listed values are for reference only; applicable limits are defined elsewhere.

Table 83 Derating Values for DDR4-2400/2666/2933/3200 tIS/tIH - AC/DC Based

△tIS, △tIH derating in [ps] AC/DC based[1]																
		CK_t, CK_c Differential Slew Rate															
		10.0V/ns		8.0V/ns		6.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1.0V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CMD, ADDR, CNTL Input Transition Rate V/ns	7.0	68	47	69	47	70	48	72	50	73	52	77	56	85	63	100	78
	6.0	66	45	67	46	68	47	69	49	71	50	75	54	83	62	98	77
	5.0	63	43	64	44	65	45	66	46	68	48	72	52	80	60	95	75
	4.0	59	40	59	40	60	41	62	43	64	45	68	49	75	56	90	71
	3.0	51	34	52	35	53	36	54	38	56	40	60	43	68	51	83	66
	2.0	36	24	37	24	38	25	39	27	41	29	45	33	53	40	68	55
	1.5	21	13	22	13	23	14	24	16	26	18	30	22	38	29	53	44
	1.0	-9	-9	-8	-8	-8	-8	-6	-6	-4	-4	0	0	8	8	23	23
	0.9	-15	-13	-15	-12	-14	-11	-12	-9	-10	-7	-6	-4	1	4	16	19
	0.8	-23	-17	-23	-17	-22	-16	-20	-14	-18	-12	-14	-8	-7	-1	8	14
	0.	-34	-23	-33	-22	-32	-21	-30	-20	-28	-18	-25	-14	-17	-6	-2	9

	7																
	0.6	-47	-31	-47	-30	-46	-29	-44	-27	-42	-25	-38	-22	-31	-14	-16	1
	0.5	-67	-42	-66	-41	-65	-40	-63	-38	-61	-36	-58	-33	-50	-25	-35	-10
	0.4	-95	-58	-95	-57	-94	-56	-92	-54	-90	-53	-86	-49	-79	-41	-64	-26

Note:

VIH/L (ac) = TBD; VIH/L (dc) = TBD; referenced to VREFCA.

15. General Reliability Parameters

Table 84 General Reliability Parameters

Parameter	Value	Notes
ESD Rating (V)	HBM: 2 kV, CDM: 500 V	
ILU	>100 mA, 1.5 × VDDmax	
MSL	3	
Reliability Level	NA	
On/Off Cycles	TBD	
Maximum PCB Assembly Reflow Cycles	3	
Machine Life (kPOH)	TBD	
LifeTime	10years	
	0.248g	
Maximum Rate of Change of External Ambient Temperature During Normal Operation (EETCRMax)	15℃/Min	

16. DDR4 Function Matrix

DDR4 SDRAM features several characteristics related to ORG and Speed support. The table below summarizes these characteristics.

Based on chip verification results, the committed specifications are shown in the table below. The following sections in this document only describe the chip's design specifications. For availability of corresponding functions, please refer to the table below.

Table 32: Function Matrix (Sorted by ORG. V: Supported, Blank: Not Supported)

Function	x8	x16	Notes
Write Leveling	V	V	

Temperature Controlled Refresh			Not Supported
Low-Power Auto Self-Refresh	V	V	MR2 A7:A6 config to be 0b10.
Fine Granularity Refresh	V	V	MR2 A8:A6 config to be 0b000. Fixed 1X mode
Multi-Purpose Register	V	V	
Data Mask	V	V	
Data Bus Inversion			Not Supported
TDQS			X8 does not support TDQS feature
ZQ Calibration	V	V	
DQ Vref Training	V	V	
Per DRAM Addressability	V	V	
Mode Register Read	V	V	
CAL	V	V	
Write CRC	V	V	
CA Parity			Not Supported
Control Gear Down Mode			
Programmable Preamble	V	V	
Maximum Power Saving Mode			
Boundary scan mode		V	Limited functionality; refer to Description of CK_t and CK_c functions; see Table 3 – DDR4 SDRAM Pin Description.
Additive Latency			
3DS			
PPR		V	x8 does not support PPR feature
Others			Refer to Section 18

Table 33 Feature Matrix (classified by speed, V: supported, blank: not supported)

Function	DLL-off Mode	DLL-on Mode			Notes
	≤ 250 Mbps	1600/1866/2133 Mbps	2400Mbps	2666/3200Mbps	
Write Leveling	V	V	V	V	
Temperature Controlled Refresh					
Low-Power Auto Self-Refresh	V	V	V	V	
Fine Granularity Refresh	V	V	V	V	
Multi-Purpose Register	V	V	V	V	

Data Mask	V	V	V	V	
Data Bus Inversion					
TDQS					
ZQ Calibration	V	V	V	V	
DQ Vref Training	V	V	V	V	
Per DRAM Addressability		V	V	V	
Mode Register Read	V	V	V	V	
CAL		V	V	V	
Write CRC		V	V	V	
CA Parity					
Control Gear Down Mode					
Programmable Preamble (= 2tCK)			V	V	
Maximum Power Saving Mode					
Boundary scan mode		V	V	V	
Additive latency					
3DS	Refer to Section 18				

17. DDR4 Operating Frequency

Speed	DDR4-3200	DDR4-2933	DDR4-2666	DDR4-2400	DDR4-2133	DDR4-1866	DDR4-1600
	22-22-22	21-21-21	19-19-19	17-17-17	15-15-15	13-13-13	11-11-11
tCK(ns)	0.625	0.682	0.75	0.833	0.937	1.071	1.25
CAS Latency (nCK)	22	21	19	17	15	13	11
tRCD(ns)	13.75	14.32	14.25	14.16	14.06	13.92	13.75
tRP(ns)	13.75	14.32	14.25	14.16	14.06	13.92	13.75
tRAS(ns)	32	32	32	32	33	34	35
tRC(ns)	45.75	46.32	46.25	46.16	47.06	47.92	48.75

18、FAQ

18.1 Recommendations for Mixed Use of Multiple Vendor Chips

It is not recommended to use this chip together with chips from other vendors. Due to significant differences in I/O characteristics among chips from different manufacturers, SI/PI issues may arise, affecting board reliability.

18.2 Description of Voltage Steps During Power-Up for VDD and VDDQ

During power-up, VDD and VDDQ transients require large currents. If the board-level power supply capability is weak or the board-level PI assessment is inadequate, a voltage dip may occur during power-up. In board design, a complete PI analysis of the power supply must be performed. The power supply module must be capable of delivering 180 mA within 400 ns.

18.3 VrefDQ Setup Procedure Requirements

Refer to the DDR4 standard specification chapter on "DQ Vref Training".

VREF must be configured in three steps according to the protocol requirements. Configuring VREF in a single step may cause errors.

Three-step procedure description (AX indicates the bits corresponding to MR6):

1) Configure A7 and A6 simultaneously.

2) A5:A0 set the Vref-DQ value in Step 2.

3) A7 = 0

18.4 Precautions for Using the s/hPPR Feature

This product only supports the Post Package Repair (PPR) feature for failed row addresses in X16 mode, even though MPR information can be obtained from X8 products (MPR0[7:6]=0b11).

The following are some precautions for using the s/hPPR feature:

1) In the third step (Guard key configuration), A6:A0 must be 0b1111111.

2) In step 6, after WL, if one of the last two beats of DQ0 is low, the PPR is considered successful.

3) In step 6, when odd parity function is enabled, the refresh command cannot be sent directly in the next precharge cycle. (The protocol sequence diagram indicates that the refresh command can be sent in the next beat.) Send refresh after the tRP interval.

4) The row addresses associated with sPPR are as follows.

Table 34 Row Addresses Associated with sPPR

sPPR Associated Row Address						
BA1	BA0	A17	A16	A15	A14	A0