Loongtion®

eMMC Storage Chip
Datasheet

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Revision History

Revision	Date	Description
Rev 1.0	2021/12/10	Release
Rev 1.1	2022/02/23	Package Dimension Change
Rev1.2	2022/09/23	Product Naming Errata Correction
Rev1.3	2023/05/23	Added 64GB pSLC product specification
Rev1.4	2023/10/07	Added BGA100 package specification
Rev1.5	2023/11/10	Added specific power consumption
Rev2.0	2024/12/05	Removed BGA100 package, removed storage temperature
Rev2.1	2024/12/05	Added wide operating temperature range, added junction temperature and thermal resistance
Rev2.2	2024/12/12	Added power-on sequence diagram
Rev2.3	2025/07/31	Updated datasheet table of contents and product physical dimension description
Rev2.4	2025/09/05	Changed pin definition diagram description
Rev2.5	2025/12/17	Changed write block misalignment field name to WRITE_BLK_MISALIGN
Rev2.5	2025/12/17	Changed package drawing dimensions D and E
Rev2.5	2025/12/17	Updated read/write power consumption reference table product capacity
Rev2.5	2025/12/17	Changed M5 attribute and direction to I/O
Rev2.5	2025/12/17	Added YIDL032MNT-S model eMMC
Rev3.0	2026/03/09	Changed model to YIDL032MNT-S eMMC
Rev3.1	2026/08/10	Added BGA100 (100FBGA) package product specification (part number TBD); errata revisions

Contents

1. Introduction 5
2. Product List 5
3. Product Features 5
    3.1 Physical Specifications 6
    3.2 Electrical Characteristics 10
4. Functional Block Diagram 11
5. Power-On Sequence 11
6. eMMC 5.1 Features 12
    6.1 Boot 12
    6.2 Sleep Mode 12
    6.3 Bus Modes 12
    6.4 Reliable Write 13
    6.5 Secure Erase 13
    6.6 Trim Function 14
    6.7 Partition Management 14
    6.8 High-Priority Interrupt (HPI) 14
    6.9 Background Operations (BKOPS) 14
    6.10 Hardware Reset (H/W Reset) 14
    6.11 Cache 15
    6.12 Dynamic Capacity Management 15
7. Registers 15
    7.1 OCR Register 15
    7.2 CID Register 15
    7.3 CSD Register 16
    7.4 Extended CSD Register 18

List of Figures

Figure 1 Physical Package Diagram....6
Figure 2 Pin Assignment Diagram....7
Figure 3 Physical Package Diagram (FBGA100)....7
Figure 4 Pin Assignment Diagram (FBGA100)....7
Figure 5 Chip Functional Block Diagram....11
Figure 6 Power-On Sequence Timing Diagram....11
Figure 7 Partition Management Diagram....14

List of Tables

Table 1 Product Ordering Information....5
Table 2 Pin Signal Description....7
Table 3 FBGA100 Package Dimension Parameters....7
Table 4 FBGA100 Pin Signal Description....7
Table 5 Read/Write Power Consumption Reference....10
Table 6 Power-On Parameter List....12
Table 7 Bus Mode Summary....13
Table 8 OCR Register....15
Table 9 CID Register Bit Definition....16
Table 10 CSD Register....16
Table 11 Extended CSD Register....18

1. **Introduction**

eMMC is an embedded flash storage solution. It combines an embedded flash controller (including LDPC-based ECC) with flash memory and a JEDEC-standard eMMC 5.1 interface. The eMMC controller (including LDPC-based ECC) manages flash memory, including ECC, wear leveling, IOPS optimization, significantly reducing the storage management burden on the host CPU.

eMMC is an ideal storage solution for many electronic devices. eMMC is designed for a wide range of applications such as smartphones, tablets, mobile phones, PDAs, handheld electronic devices, digital cameras, multimedia devices, and more. With its compact size, low power consumption, and many enhanced features, it is not only used in consumer products but also rapidly and widely adopted in embedded applications, such as numerous computer-side module designs.

2. Product List

Table 1 Product Ordering Information

Capacity	Product Part Number	Flash Type	Temperature Range	Package Type
8GB	YMDL008MNS-S	pSLC	-55℃~95℃	153FBGA
16GB	YMDL016MNS-S			
32GB	YMDL032MNS-S			
64GB	YMDL064MNS-S			
32GB	YIDL032MNT-S	TLC	-40℃~85℃	
64GB	YIDL064MNT-S			
128GB	YIDL128MNT-S			
256GB	YIDL256MNT-S			
32GB	TBD	pSLC	-55~125℃	100FBGA

Note: BGA100 (100FBGA) packaged products are a newly added specification. Part numbers (PN) and capacities are to be confirmed and will be updated in this table. See Section 3.1.2 for details.

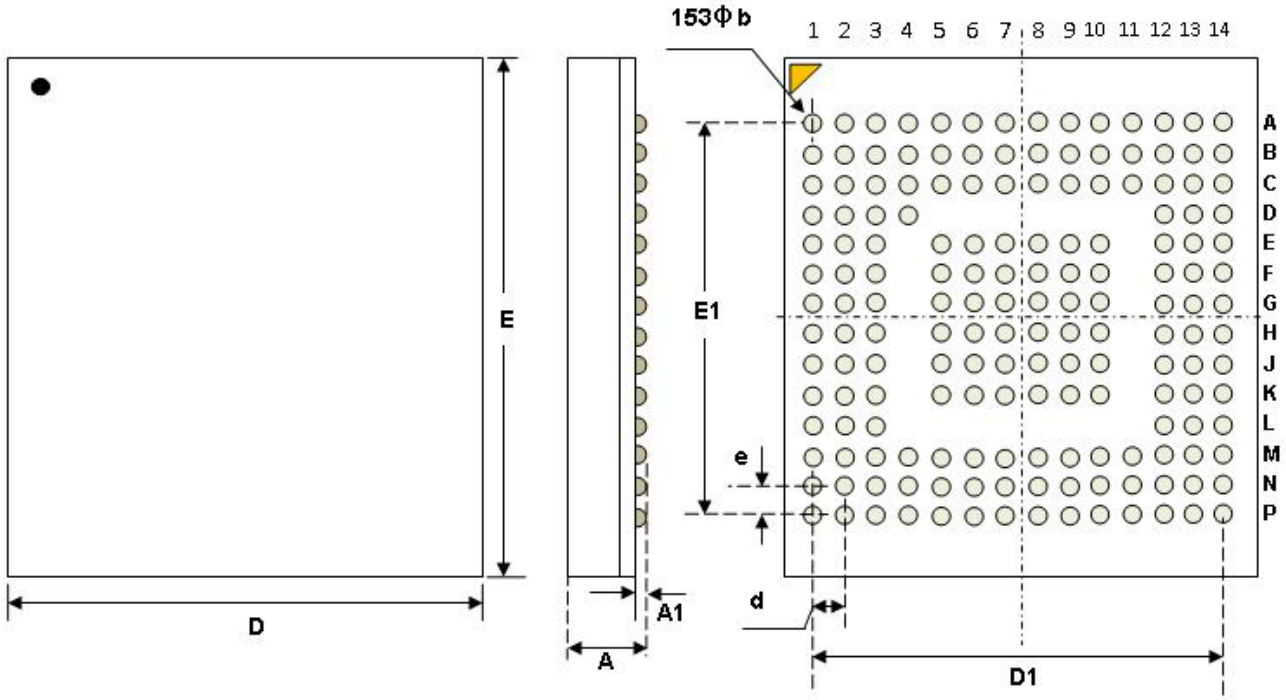
3. Product Features

- Compliant with eMMC 5.1 standard;
- Supports 3.3V/1.8V supply;
- Supports 12-line bus (CLK, CMD, Data Strobe, Data Bus, and RST_n);
- Supports clock frequency up to 200MHz (HS400 mode);
- Supports Single Data Rate (SDR) and Double Data Rate (DDR);
- Supports different bus widths: 1-bit, 4-bit, 8-bit;
- Supports RPMB;
- Supports multiple partitions with enhanced attributes;
- Supports lock/unlock and write protection;
- Supports data protection on power failure;
- Supports High-Priority Interrupt (HPI);
- Supports Dynamic Power Manager: standby and sleep modes;
- Supports command queuing;
- Supports secure write protection;

3.1 Physical Specifications

3.1.1 FBGA153 Package Physical Characteristics

- Physical Dimensions: 11.5mm x 13.0mm x 1.0mm;



Dimension Symbol	Value (mm)			Dimension Symbol	Value (mm)		
	Min	Nom	Max		Min	Nom	Max
D	-	11.5	-	D1	-	6.5	-
E	-	13	-	E1	-	6.5	-
A	-	1.0	1.1	A1	-	0.08	-
d	-	0.5	-	e	-	0.5	-
b	0.25	0.3	0.35				

Figure 1 Physical Package Diagram

- Pin Assignment

Pin top view (Top View, Ball Down) is shown below:

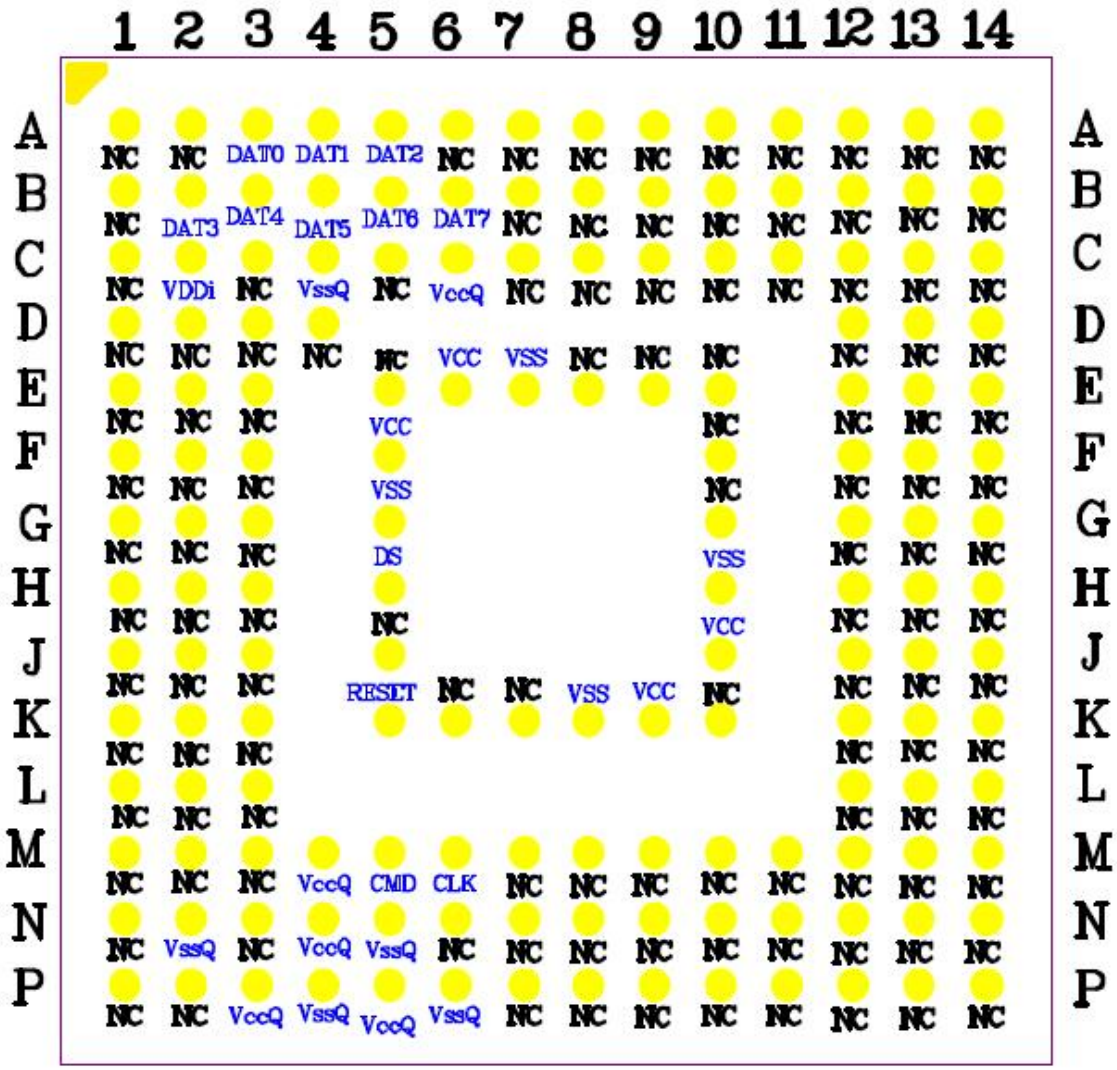


Figure 2 Pin Assignment Diagram

- Pin Signal Description

Table 2 Pin Signal Description

Pin No.	Signal Name	Type	Pin Function
M6	CLK	Input	eMMC clock input signal; used to sample command and data signals on each clock cycle.
M5	CMD	I/O	The eMMC command/response signal is bidirectional; the host sends commands to the eMMC, and the eMMC sends responses to the host. The command signal has two operating modes: open-drain output during initialization (a 4.7 kΩ pull-up resistor to VCCQ is recommended), and push-pull output after initialization.
A3,A4,A5 A3, A4, A5, B2, B3, B4, B5, B6	DAT0-DAT7	I/O	8-bit data transfer signal, bidirectional; during initialization, DAT0 is open-drain output (a 10 kΩ pull-up resistor to VCCQ is recommended), and after initialization it is configured as push-pull output.

K5	RST_n	Input	Hardware reset input (disabled by default).
E6, F5, J10, K9	V_{CC}	Power	NAND flash core power supply: 2.7V to 3.6V.
C6, M4, N4, P3, P5	V_{CCQ}	Power	Interface power supply, supports two voltage ranges: High voltage (low-speed mode): 2.7V~3.6V; Low voltage (high-speed mode): 1.7V~1.95V.
E7, G5, H10, K8	V_{SS}	GND	Ground signal.
C4, N2, N5, P4, P6	V_{SSQ}	GND	Ground signal.
C2	VDDi	O	Controller core power, supplied by internal LDO; connect a 0.1μF to 2.2μF capacitor to ground externally.
H5	DS	O	DS output signal, enabled after configuration in HS400 mode, used for data synchronization with the host; frequency is the same as CLK.

3.1.2 FBGA100 Package Physical Characteristics

- Physical Dimensions: 14.0mm x 18.0mm x 3.0mm;

Figure 3 Physical Package Diagram (FBGA100)

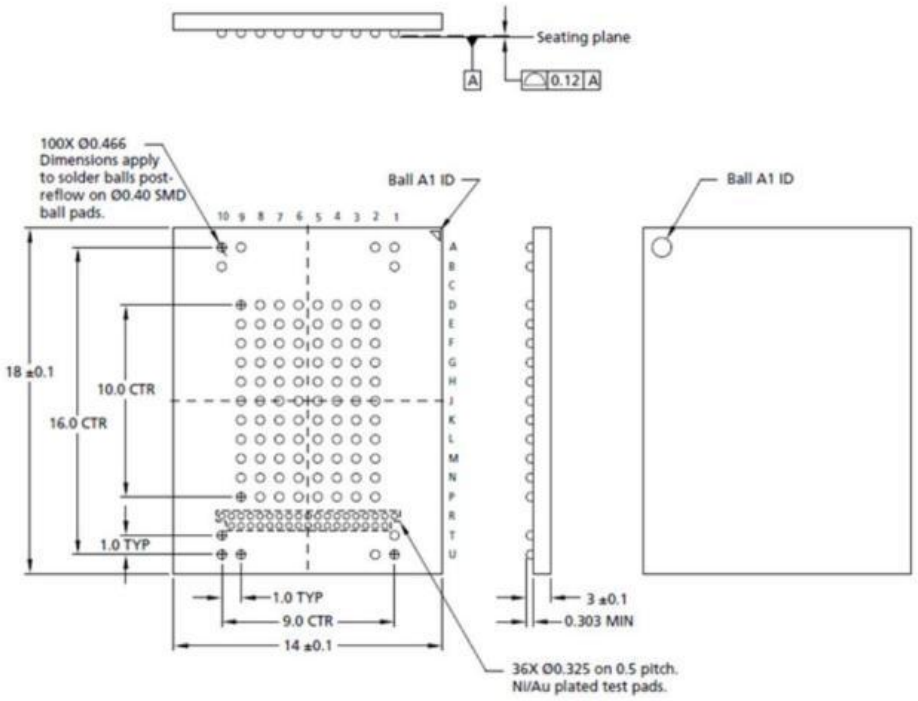


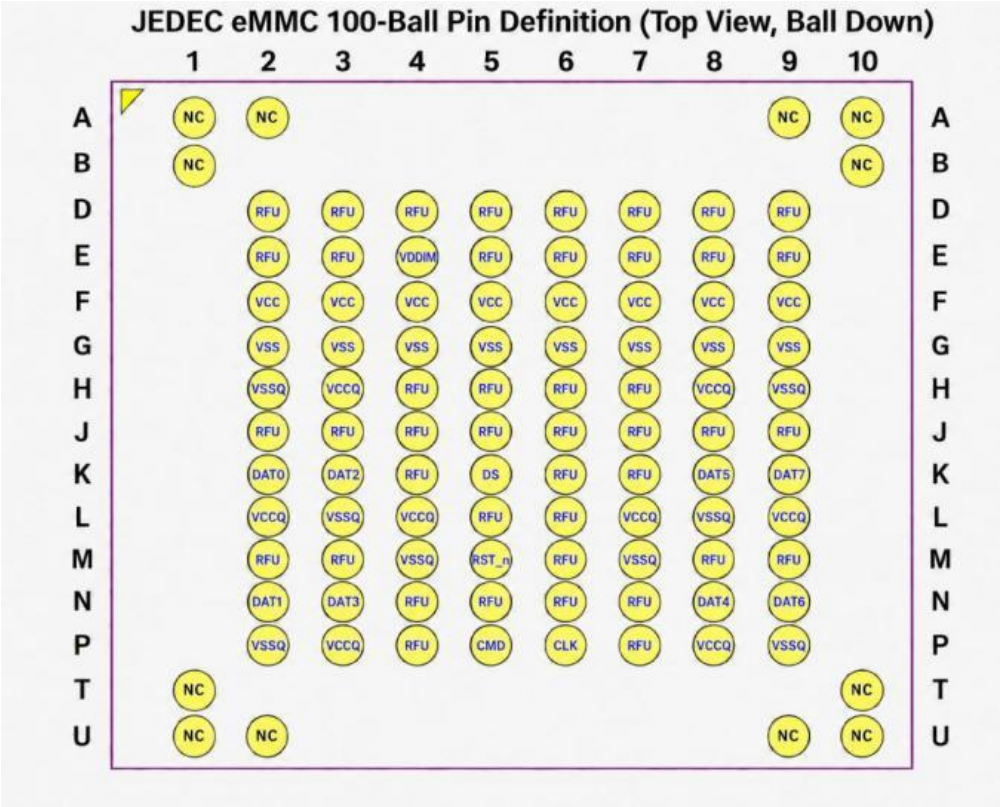
Table 3 FBGA100 Package Dimension Parameters

Dimension Symbol	Value (mm)	Value (mm)	Value (mm)	Dimension Symbol	Value (mm)	Value (mm)	Value (mm)
Dimension Symbol	Min	Nom	Max	Dimension Symbol	Min	Nom	Max
D	-	18.0	-	D1	-	16.0	-
D2	-	10.0	-	E	-	14.0	-
E1	-	6.5	-	A	-	3.0	3.1
A1	-	0.08	-	d	-	0.5	-
e	-	0.5	-				

- Pin Assignment

Pin top view (Top View, Ball Down) is shown below:

Figure 4 Pin Assignment Diagram (FBGA100)



- Pin Signal Description

Table 4 FBGA100 Pin Signal Description

100-Ball Device	symbol	Type	Ball Function
P6	CLK	Input	Clock input signal. Controls the transmission on the command line and data lines on each clock cycle.
P5	CMD	I/O	Command/response signal. The host sends commands through this line, and the device returns responses through this line.
K2	DATA0	I/O	Data bit 0. DAT0 is used first for data transfer by default after power-on or reset.
N2	DATA1	I/O	Data bit 1. Used for data transfer in 4-bit/8-bit bus modes.
K3	DATA2	I/O	Data bit 2. Used for data transfer in 4-bit/8-bit bus modes.
N3	DATA3	I/O	Data bit 3. Used for data transfer in 4-bit/8-bit bus modes.
N8	DATA4	I/O	Data bit 4. Used for data transfer in 8-bit bus mode.
K8	DATA5	I/O	Data bit 5. Used for data transfer in 8-bit bus mode.
N9	DATA6	I/O	Data bit 6. Used for data transfer in 8-bit bus mode.
K9	DATA7	I/O	Data bit 7. Used for data transfer in 8-bit bus mode.
M5	RST_n	Input	Hardware reset input, active low.
F2, F3, F4, F5, F6, F7, F8, F9	VCC	Supply	NAND flash core power supply (2.7V~3.6V).
H3, H8, L2, L4, L7, L9, P3, P8	VCCQ	Supply	eMMC controller core and eMMC interface I/O power supply.

G2, G3, G4, G5, G6, G7, G8, G9	VSS	Ground	Ground signal.
H2, H9, L3, L8, M4, M7, P2, P9	VSSQ	Ground	Ground signal.
E4	VDDIM	Power / Internal node	Internal voltage node; connect a 1μF decoupling capacitor to ground externally.
K5	DS	I/O	Data Strobe signal, mainly used for data sampling and timing synchronization in HS400 mode.

3.2 Electrical Characteristics

- Operating Voltage Range:

  VCC = 2.7V~3.6V (typical 3.3V);

  V_{CCQ}= 1.7V~1.95V(typical 1.8V), 2.7V~3.6V (typical 3.3V)；

- Read/Write Power Consumption

Table 5 Read/Write Power Consumption Reference

Product Capacity	Operation Mode	Read (mA)		Write (mA)	
		I_{CC}	I_{CCQ}	I_{CC}	I_{CCQ}
YMDL008MNS-S	HS400	50	70	30	50
YMDL016MNS-S		55	95	45	95
YMDL032MNS-S		60	120	45	110
YIDL032MNT-S					
YMDL064MTS-S		75	150	60	130
YIDL064MNT-S		55	95	45	95
YIDL128MNT-S		60	120	45	110
YIDL256MNT-S		75	150	60	130

- Operating Temperature:

  Industrial Grade: -40 to 85°C;

  Extended Temperature: -55 to 95°C;

  BGA100 (100FBGA) Package: -55 to 125°C;

- Temperature Parameters:

  Junction Temperature: Tj max 115°C;

  Thermal Resistance: 35°C/W;

- Others: RoHS compliant.

4. Functional Block Diagram

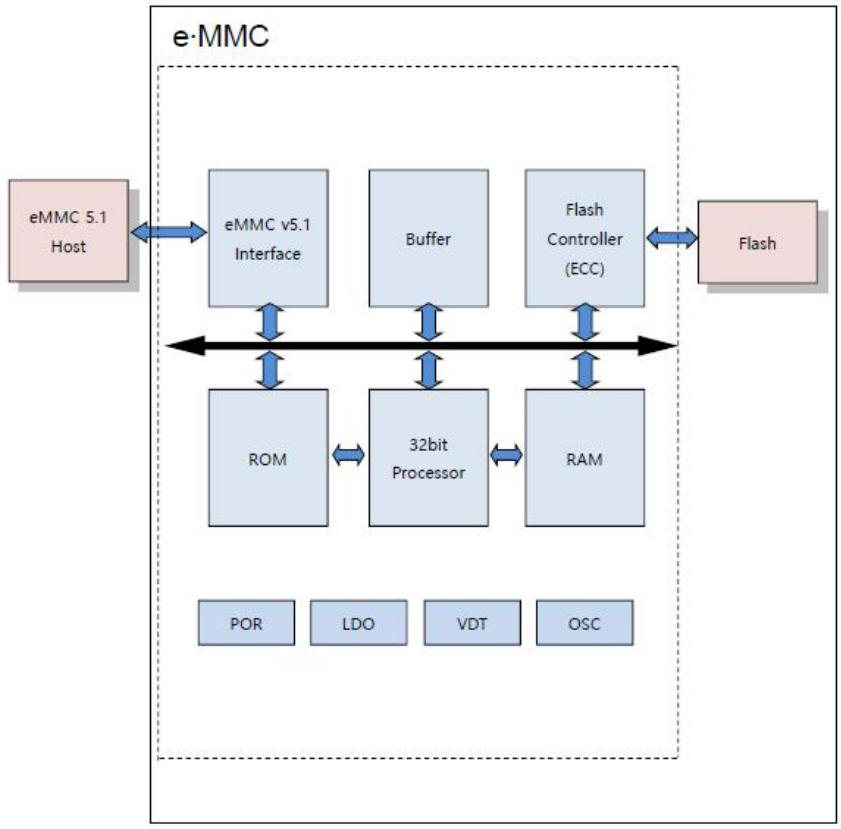


Figure 5 Chip Functional Block Diagram

5. Power-On Sequence

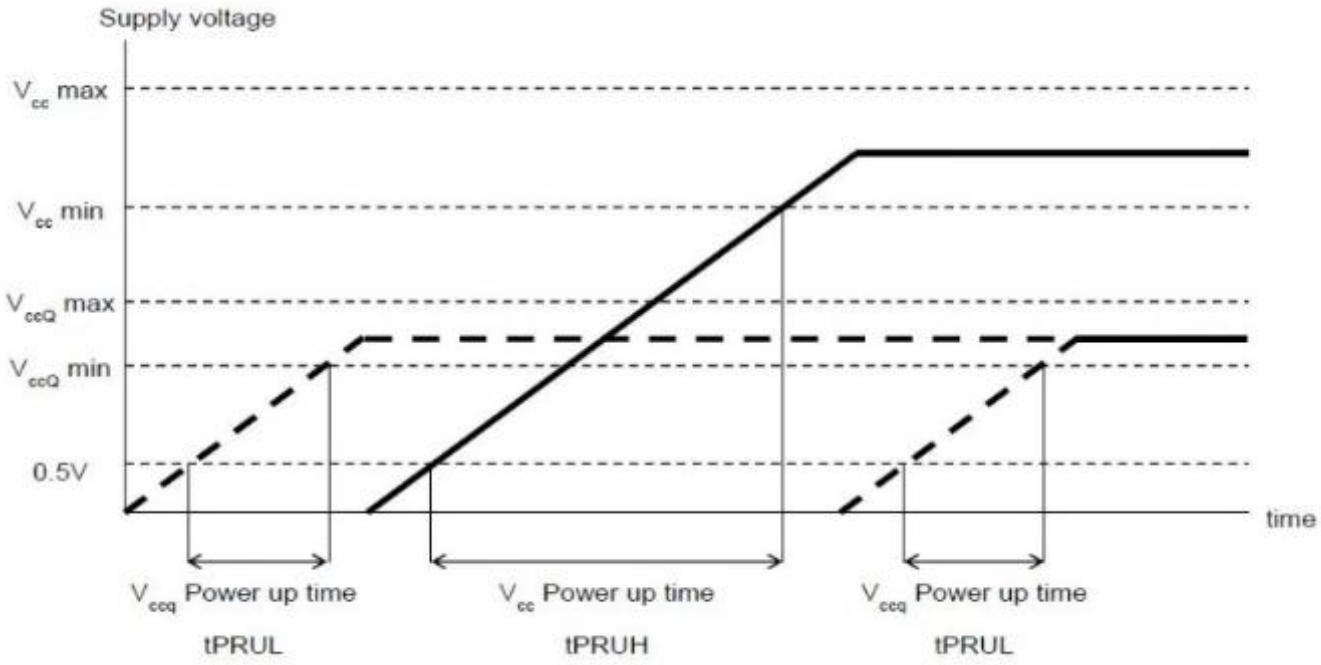


Figure 6 Power-On Sequence Timing Diagram

Table 6 Power-On Parameter List

Parameter	Symbol	Min	Max
V_{CC}=3.3V	t_{PRUH}	5us	35ms
V_{CCQ} =1.8V	t_{PRUL}	5us	25ms

6. eMMC 5.1 Features

6.1 Boot

eMMC supports JESD84-B51A boot operation mode, supporting mandatory Boot mode and alternate Boot mode.

6.2 Sleep Mode

The device can switch between sleep state and standby state via Sleep/Awake (CMD5). In sleep state, the storage device power consumption is minimized. In this state, the storage device only responds to reset commands (CMD0 with argument 0x00000000 or 0xF0F0F0F0, or hardware reset) and Sleep/Awake commands (CMD5). All other commands are ignored. VCC power may be switched off in sleep state to further save system power.

For more information, refer to JESD84-B51A.

6.3 Bus Modes

- Boot Mode

After power-on reset, receiving CMD0 with argument 0xF0F0F0F0, or hardware reset signal being asserted, the device enters boot mode.

- Device Identification Mode

After boot operation mode is completed, or if the host and/or device do not support boot operation mode, the device enters device identification mode until the SET_RCA command (CMD3) is received.

- Interrupt Mode

Host and device can enter interrupt mode, and the host controls exit. In interrupt mode, no data transfers occur. The only allowed message is an interrupt service request from the device or host.

- Data Transfer Mode

Once an RCA is assigned, the device enters data transfer mode. After identifying the device on the bus, the host enters data transfer mode.

- Inactive Mode

If the device operating voltage range or operation mode is invalid, the device enters inactive mode. The device can also enter inactive mode with the GO_INACTIVE_STATE command (CMD15). The device is reset to pre-idle state after power-on.

Table 7 Bus Mode Summary

Device State	Operation Mode	Bus Mode
Inactive State	Inactive Mode	Open-drain
Pre-Idle State	Boot Mode	
Pre-Boot State		
Idle State	Device Identification Mode	
Identification State		
Stand-by State		
Sleep State	Data Transfer Mode	Push-pull
Transfer State		
Bus-Test State		
Send Data State		
Receive Data State		
Programming State		
Disconnect State		
Boot State	Boot Mode	
Wait-IRQ State	Wait-IRQ Mode	Open-drain

6.4 Reliable Write

Per the eMMC 5.1 specification, the eMMC supports 512-byte reliable write.

Reliable write is a special write mode in which the old data pointed to by a logical address must remain unchanged until new data written to the same logical address is successfully programmed. This ensures that the target address will not contain undefined data when updated. Data remains valid even if power is lost during programming of a reliable write.

6.5 Secure Erase

In addition to standard erase commands, eMMC supports optional secure erase commands.

Secure erase differs from basic erase in that it requires the device and host to wait for the operation to complete before moving to the next device operation.

For more information, refer to JESD84-B51A.

The secure erase command requires the device to perform a secure purge on erase groups and replicate the items identified for erase within those erase groups. The purge operation is defined as overwriting the addressable location with a single character and performing the erase.

The purge operation is defined as overwriting the addressable location with a single character and performing the erase.

This new command satisfies the requirements of high-security applications: once data is erased, it can no longer be retrieved from the device.

6.6 Trim Function

The Trim function is similar to the Erase command, but applies the erase operation to write blocks rather than erase groups.

For more information, refer to JESD84-B51A.

6.7 Partition Management

The default regions of the device include a user data area for data storage, two possible boot areas for booting, and an authenticated and protected RPMB partition. The initial memory configuration (before any partition operations) includes the user data area, RPMB partition, and boot partitions.

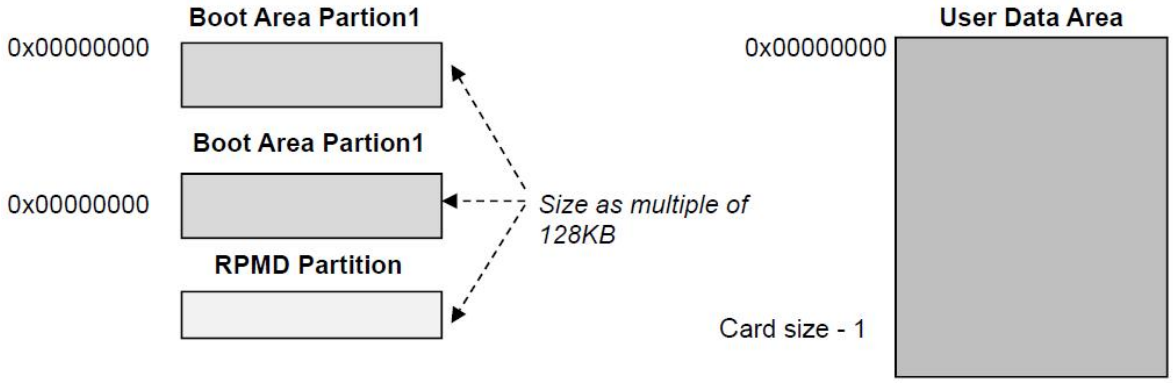


Figure 7 Partition Management Diagram

6.8 High-Priority Interrupt (HPI)

Many operating systems use demand paging to start user-requested processes. If the host needs to fetch a page during a continuous operation, the request is delayed until the write command completes, which can take up to 350 ms in the worst case.

The High-Priority Interrupt (HPI) defined in JESD84-B51A achieves low read latency by pausing a low-priority operation before it actually completes. This mechanism can reduce read latency to 5 ms in typical cases.

For more information, refer to JESD84-B51A.

6.9 Background Operations (BKOPS)

The device needs to perform various internal maintenance operations, such as garbage collection, erase, and compaction. To reduce latency during time-critical operations, maintenance should be performed when the device is not serving the host.

Operations are then divided into two types: foreground operations (such as read or write commands) and background operations (operations the device can perform when the host is not being served).

For more information, refer to JESD84-B51A.

6.10 Hardware Reset (H/W Reset)

The host can reset the device using the hardware reset (RST_n pin). During device reset, the RST_n pin should be held low and released after reset completes. Power-on write-protected block status is not affected.

6.11 Cache

Cache is temporary storage space in the eMMC device. In typical cases, cache reduces write and read access time. The host cannot access the cache directly. The cache can also be used for specific operations, such as execution memory for the memory controller based on the LDPC error-correction algorithm and/or as storage for the address mapping table, but its definition is beyond the scope of this specification.

For more information, refer to JESD84-B51A.

6.12 Dynamic Capacity Management

Heavy memory usage and flash aging can cause bad blocks. Dynamic capacity management provides a mechanism for the storage device to maintain capacity and extend device life by replacing bad blocks.

The mechanism for dynamic capacity operation is based on memory array partitioning and WP group granularity. Capacity can be reduced by releasing any WP group in the user area address space. A released WP group acts as a permanent write-protected group and should not be read from: writing to an address within a released WP group returns a WP error; reading the address header of a released WP group may return an error; when checking write protection (CMD30) and write protection type (CMD31), protected groups and permanent write protection should be reported accordingly.

For more information, refer to JESD84-B51A.

7. Registers

7.1 OCR Register

The 32-bit Operation Conditions Register (OCR) stores the device supply voltage (VDD) and access mode information. In addition, the register includes status information bits. This status bit is set if the device startup process has completed. All devices support the OCR.

Table 8 OCR Register

OCR Bit	VCCQ Voltage Range	Default Value (Description)	Notes
[6:0]	Reserved	000 0000b	
[7]	1.70 ~ 1.95V	1b	
[14:8]	2.0 ~ 2.6V	000 0000b	
[23:15]	2.7 ~ 3.6V	1 1111 1111b	
[28:24]	Reserved	0 0000b	
[30:29]	Access mode	10b	
[31]	Card power-up status bit (busy)		

Note: [31] If the device has not completed power-up initialization, this bit is low (0).

7.2 CID Register

The CID register is a device identification register, 128 bits wide, containing device identification information used during the device identification phase (protocol).

Every flash or I/O device should have a unique identification code. eMMC devices have a unique identification code (CID).

The following table lists the device identification register structure definition for eMMC products.

Table 9 CID Register Bit Definition

Name	Register Name	Width	CID Bit Field	CID Value	Notes
Manufacturer ID	MID	8	[127:120]	FFh	
Reserved		6	[119:114]		
Card/BGA Type	CBX	2	[113:112]	01	BGA
OEM/User ID	OID	8	[111:104]	FFh	Not fixed
Product Name	PNM	48	[103:56]	FFFFFFh	
Product Revision	PRV	8	[55:48]	FFh	Not fixed
Product Serial Number	PSN	32	[47:16]	Random by production	Not fixed
Manufacturing Date	MDT	8	[15:8]	Month，year	Not fixed
CRC7 Checksum	CRC	7	[7:1]	00h	Not fixed
Reserved	-	1	[0:0]	1h	

7.3 CSD Register

The CSD (Card Specific Data Register) register provides information on how to access the eMMC content. This register defines data format, error correction type, maximum data access time, data transfer speed, DSR register availability, and more. The programmable part of the register (entries marked W or E, see below) can be changed by CMD27. Entry type encodings in the table are as follows:

R: Read only;

W: Write once, not readable;

R/W: Write once, readable;

W/E: Writable multiple times, not readable; value unchanged after power-off, H/W reset, or CMD0 reset;

R/W/E: Writable multiple times, readable; value unchanged after power-off, H/W reset, or CMD0 reset;

R/W/C_P: Readable and writable; value cleared after power-off, H/W reset, or CMD0 reset;

R/W/E_P: Writable multiple times, readable; value reset after power-off, H/W reset, or CMD0 reset;

W/E/P: Writable multiple times, not readable; value reset after power-off, H/W reset, or CMD0 reset;

Table 10 CSD Register

Name	Field Name	Width	Access Type	CSD Bit	CSD Value	Notes
CSD Structure	CSD_STRUCTURE	2	R	[127:126]	3h	
System Specification Version	SPEC_VERS	4	R	[125:122]	4h	
Reserved	-	2	R	[121:120]		
Data Read Access Time	TAAC	8	R	[119:112]	2Fh	20ms
Data read access time in CLK cycles \(NSAC×100\)	NSAC	8	R	[111:104]	1h	
Maximum Bus Clock Frequency	TRAN_SPEED	8	R	[103:96]	2Ah	20MHz
Device Command Classes	CCC	12	R	[95:84]	5F5h	Class 0, 2,4,5,6,7, 8,10

Maximum Read Data Block Length	READ_BL_LEN	4	R	[83:80]	9h	512B
Partial Blocks for Read Allowed	READ_BL_PARTIAL	1	R	[79:79]	0h	Not supported Write Block Misalignment
Write Block Misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h	Not supported Read Block Misalignment
Read Block Misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h	Not supported DSR Implemented
DSR Implemented	DSR_IMP	1	R	[76:76]	0h	Not supported Reserved
Reserved		2	R	[75:74]		
Device Capacity	C_SIZE	12	R	[73:62]	FFFh	
Maximum read current at VDD min	VDD_R_CURR_MIN	3	R	[61:59]	6h	
Maximum read current at VDD max	VDD_R_CURR_MAX	3	R	[58:56]	6h	
Maximum write current at VDD min	VDD_W_CURR_MIN	3	R	[55:53]	6h	
Maximum write current at VDD max	VDD_W_CURR_MAX	3	R	[52:50]	6h	
Device Capacity Multiplier	C_SIZE_MULT	3	R	[49:47]	7h	
Device Capacity Multiplier	ERASE_GRP_SIZE	5	R	[46:42]	1Fh	
Erase Group Size Multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh	
Write Protect Group Size	WP_GRP_SIZE	5	R	[36:32]	1h	
Write Protect Group Enable	WP_GRP_ENABLE	1	R	[31:31]	1h	
Device Default ECC	DEFAULT_ECC	2	R	[30:29]	0h	
Read/Write Speed Factor	R2W_FACTOR	3	R	[28:26]	1h	
Maximum Write Data Block Length	WRITE_BL_LEN	4	R	[25:22]	9h	512B
Partial Block Write Allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h	Not supported Reserved
Reserved		4	R	[20:17]		
Content Protection Application	CONTENT_PROT_APP	1	R	[16:16]	0h	Not supported File Format Group
File Format Group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h	
Copy Flag	COPY	1	R/W	[14:14]	0h	
Permanent Write Protect	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h	
Temporary Write Protect	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h	
File Format	FILE_FORMAT	2	R/W	[11:10]	0h	
ECC Value	ECC	2	R/W/E	[9:8]	0h	None
CRC	CRC	7	R/W/E	[7:1]	Dh	
Reserved, always 1		1	-	[0:0]	1h	

The following sections describe the CSD fields and related data types. If not explicitly defined, all bit strings are defined as binary-coded numbers starting from the most significant bit.

7.4 Extended CSD Register

The Extended CSD register defines eMMC attributes and selected modes, 512 bytes in length. The upper 320 bytes are attribute fields defining the eMMC capacity; the host cannot modify them. The lower 192 bytes are mode fields defining the current eMMC configuration. The host can modify these configurations via the SWITCH command.

R: Read only;

W: Write once, not readable;

R/W: Write once, readable;

W/E: Writable multiple times, not readable; value unchanged after power-off, H/W reset, or CMD0 reset;

R/W/E: Writable multiple times, readable; value unchanged after power-off, H/W reset, or CMD0 reset;

R/W/C_P: Readable and writable; value cleared after power-off, H/W reset, or CMD0 reset;

R/W/E_P: Writable multiple times, readable; value reset after power-off, H/W reset, or CMD0 reset;

W/E_P: Writable multiple times, not readable; value reset after power-off, H/W reset, or CMD0 reset;

Table 11 Extended CSD Register

Name	Field Name	Cell Type	CSD Bit	CSD Value	Notes
Reserved	RESERVED	TBD	[511:506]		
Extended Secure Erase	EXT_SECURITY_ERR	R	[505]	0h	Only for eMMC 4.5 (JESD84-B51A)
Supported Command Sets	S_CMD_SET	R	[504]	1h	Assigned by MMCA
Bit[1]=1: HPI mechanism implementation based on CMD12; Bit[1]=0: HPI mechanism implementation based on CMD13; Bit[0]=1: HPI mechanism supported; Bit[0]=0: HPI mechanism not supported	HPI_FEATURES	R	[503]	3h	Bit[1]=1: HPI mechanism implementation based on CMD12 Bit[1]=0: HPI mechanism implementation based on CMD13 Bit[0]=1: HPI mechanism support Bit[0]=0: HPI mechanism not supported (default)
Background Operations Support	BKOPS_SUPPORT	R	[502]	1h	Supported
Max Packed Read Commands	MAX_PACKED_READS	R	[501]	3Fh	

Max Packed Write Commands	MAX_PACKED_WRITES	R	[500]	3Fh	
Data Tag Support	DATA_TAG_SUPPORT	R	[499]	1h	Supported
Tag Unit Length	TAG_UNIT_SIZE	R	[498]	1h	1024Bytes
Tag Resource Size	TAG_RES_SIZE	R	[497]	0h	
Context Management Capabilities	CONTEXT_CAPABILITIES	R	[496]	5h	
Large Unit Size	LARGE_UNIT_SIZE_M1	R	[495]	0h	
Extended Partition Attribute Support	EXT_SUPPORT	R	[494]	3h	
Supported Modes	SUPPORTED_MODES	R	[493]	1h	
FFU Functionality	FFU_FEATURES	R	[492]	1h	
Operation Code Timeout	OPERATION_CODE_TIMEOUT	R	[491]	17h	
FFU Parameters	FFU_ARG	R	[490:487]	0h	
Barrier Support	BARRIER_SUPPORT	R	[486]	0h	
Reserved		TBD	[485:309]		
Command Queue Support	CMDQ_SUPPORT	R	[308]	0h	
Command Queue Depth	CMDQ_DEPTH	R	[307]	0h	
Reserved		TBD	[306]		
Number of Correctly Programmed Firmware Sectors	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	R	[305:302]	0h	
Vendor Proprietary Health Report	VENDOR_PROPRIETARY_HEALTH_REPORT	R	[301:270]	0h	
Device Life Time Estimation Type B	DEVICE_LIFE_TIME_EST_TYP_B	R	[269]	1h	
Device Life Time Estimation (Type A)	DEVICE_LIFE_TIME_EST_TYP_A	R	[268]	1h	
Pre-End of Life Information	PRE_EOL_INFO	R	[267]	1h	
Optimal Read Size	OPTIMAL_READ_SIZE	R	[266]	8h	

Optimal Write Size	OPTIMAL_WRITE_SIZE	R	[265]	8h	
Optimal TRIM Unit Size	OPTIMAL_TRIM_UNIT_SIZE	R	[264]	8h	
Device Version	DEVICE_VERSION	R	[263:262]	0h	
Firmware Version	FIRMWARE_VERSION	R	[261:254]	---	
200MHz, DDR 3.6V Power Class	PWR_CL_DDR_200_360	R	[253]	0h	
Cache Size	CACHE_SIZE	R	[252:249]	100h	
Generic CMD6 Timeout	GENERIC_CMD6_TIME	R	[248]	32h	Undefined
Power-Off Notification \(Long\) Timeout	POWER_OFF_LONG_TIME	R	[247]	3Ch	Undefined
Background Operations Status	BKOPS_STATUS	R	[246]	0h	None (no operation pending)
Correctly programmed sectors number	CORRECTLY_PRG_SECTORS_NUM	R	[245:242]	0h	
Initialization time after partitioning	INI_TIMEOUT_AP	R	[241]	1Eh	Initial time out 3sec
Cache Flush Policy	CACHE_FLUSH_POLICY	R	[240]	0h	
52MHz, DDR 3.6V Power Class	PWR_CL_DDR_52_360	R	[239]	0h	
52MHz, DDR 1.95V Power Class	PWR_CL_DDR_52_195	R	[238]	0h	
200MHz 1.95V power class	PWR_CL_200_195	R	[237]	0h	
200MHz 1.30V power class	PWR_CL_200_130	R	[236]	0h	
Performance	MIN_PERF_DDR_W_8_52	R	[235]	0h	
Performance	MIN_PERF_DDR_R_8_52	R	[234]	0h	
Reserved	RESERVED	TBD	[233]		
TRIM_MULT	TRIM_MULT	R	[232]	2h	TRIM timeout = 300 ms × 2 = 600 ms
Security Feature Support	SEC_FEATURE_SUPPORT	R	[231]	55h	Support the sanitize operation Supports secure and insecure trim operation Support the auto erase on retired defective portion of array

					Supports secure purge operations
Secure Erase Timeout Multiple	SEC_ERASE_MULT	R	[230]	1Bh	Secure Erase Timeout= 5.1 sec
Multi-Sector TRIM	SEC_TRIM_MULT	R	[229]	11h	Secure Trim Timeout= 8.1 sec
Boot Information	BOOT_INFO	R	[228]	7h	Bit[2]=1: Device supports high speed timing during boot Bit[1]=1: Device supports dual data rate during boot Bit[0]=1: Device supports alternate boot method Bit[0,1,2]=0: Does not support each feature; Bit[7:3] Reserved
Reserved	RESERVED	TBD	[227]		
Boot Partition Size Multiple	BOOT_SIZE_MULT	R	[226]	20h	
Access Size	ACC_SIZE	R	[225]	6h	
High Capacity Erase Group Size	HC_ERASE_GRP_SIZE	R	[224]	1h	
Erase Timeout Multiplier	ERASE_TIMEOUT_MULT	R	[223]	1h	High Capacity erase timeout : 300ms
Reliable Write Sector Count	REL_WR_SEC_C	R	[222]	1h	1sector
High Capacity Write Protect Group Size	HC_WP_GRP_SIZE	R	[221]	20h	
Sleep Current \(VCC\)	S_C_VCC	R	[220]	7h	Sleep current: 128uA
Sleep Current \(VCCQ\)	S_C_VCCQ	R	[219]	7h	Sleep current: 128uA
Production State Awareness Timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	R	[218]	17h	
Sleep/Wakeup Timeout	S_A_TIMEOUT	R	[217]	17h	Sleep/Awake Timeout: 85 ms
Sleep Notification Time	SLEEP_NOTIFICATION_TIME	R	[216]	11h	
Sector Count	SEC_COUNT	R	[215:212]	---	64GB: 747C000h
Secure Write Protection Info	SECURE_WP_INFO	TBD	[211]	0h	
8-bit 52 MHz Minimum Write Performance	MIN_PERF_W_8_52	R	[210]	0h	
8-bit 52 MHz Minimum Read Performance	MIN_PERF_R_8_52	R	[209]	0h	

Write Performance	MIN_PERF_W_8_26_4_52	R	[208]	0h	
Read Performance	MIN_PERF_R_8_26_4_52	R	[207]	0h	
4-bit 26 MHz Minimum Write Performance	MIN_PERF_W_4_26	R	[206]	0h	
4bit 26MHz Minimum Read Performance	MIN_PERF_R_4_26	R	[205]	0h	
Reserved	RESERVED	R	[204]		
26MHz 3.6V 1R Power Class	PWR_CL_26_360	R	[203]	0h	Max RMS Current = 100 mA, Max Peak Current = 200 mA
52MHz 3.6V 1R Power Class	PWR_CL_52_360	R	[202]	0h	MAX RMS Current = 100mA, MAX Peak Current = 200mA
26MHz 1.95V 1R Power Class	PWR_CL_26_195	R	[201]	0h	MAX RMS Current = 65mA, MAX Peak Current = 130mA
2MHz 1.95V 1R Power Class	PWR_CL_52_195	R	[200]	0h	MAX RMS Current = 65mA, MAX Peak Current = 130mA
Partition Switching Time	PARTITION_SWITCH_TIME	R	[199]	5h	Partition switch time : 10ms
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	R	[198]	19h	HPI time out : 20ms
I/O Driver Strength	DRIVER_STRENGTH	R	[197]	Fh	Supports driver strength: Type0, Type1, Type2, Type3
Device Type	DEVICE_TYPE	R	[196]	57h	1. HS400 @1.8V High-speed Data Rate 52@1.8V/3.3V High-speed Data Rate 52@rated device voltage(s) High-speed Data Rate 26@rated device voltage(s)
Reserved	RESERVED	TBD	[195]		
CSD Structure	CSD_STRUCTURE	R	[194]	2h	System Specification Version
Reserved	RESERVED	TBD	[193]		
EXT_CSD Revision	EXT_CSD_REV	R	[192]	8h	Version 1.8 (MMC v5.1)
Mode Segment					
Command Set	CMD_SET	R/W/ E_P	[191]	0h	
Reserved	RESERVED	TBD	[190]		

Command Set Version	CMD_SET_REV	R	[189]	0h	V4.0
Reserved	RESERVED	TBD	[188]		
Power class	POWER_CLASS	R/W/ E_P	[187]	0h	High-speed interface timing
Reserved	RESERVED	TBD	[186]		
High-speed interface timing	HS_TIMING	R/W/ E_P	[185]	0h	Depends on host interface speed. Default is 0, but it can be set to 1 by the host.
STROBE support	STROBE_SUPPORT	R	[184]	1h	
Bus width mode	BUS_WIDTH	W/E_P _P	[183]	0h	
Reserved	RESERVED		[182]		
Erased memory content	ERASED_MEM_CONT	R	[181]	0h	0 after erase
Reserved	RESERVED	TBD	[180]		
Partition Configuration	PARTITION_CONFIG	R/W/E & R/W/E_P /E_P	[179]	0h	
Boot Configuration Protection	BOOT_CONFIG_PROT	R/W/E & R/ W /C_P	[178]	0h	
Reserved	BOOT_BUS_CONDITIONS	R/W /E	[177]	0h	
Reserved1	RESERVED	TBD	[176]		
Erase Group Definition	ERASE_GROUP_DEF	R	[175]	0h	
Boot Write Protection Status Register		TBD	[174]	0h	
Boot Area Write Protection Register	BOOT_WP	R/W/E & R/ W /C_P	[173]	0h	Bit[6]=0 : Master is permitted to set B_PWR_WP_EN (bit0) Bit[4]=0 : Master is permitted to set B_PERM_WP_EN (bit2) Bit[2]=0 : Boot Region is not permanently write protected Bit[0]=0 : Boot Region is not power-on write protected
Reserved	RESERVED	TBD	[172]		

User Area Write Protection Register	USER_WP	R/W, & R/W /C_P & RW/E_P /E_P	[171]	0h	
Reserved	RESERVED	TBD	[170]		
FW Configuration	FW_CONFIG	R/W	[169]	0h	FW update enabled
RPMB Size	RPMB_SIZE_MULT	R	[168]	20h	RPMB size 4MB
Write Reliability Setting Register	WR_REL_SET	R/W	[167]	0h	
Write Reliability Parameter Register	WR_REL_PARAM	R	[166]	14h	Enhances the definition of reliable write; all WR_DATA_REL bits in the WR_REL_SET register are R/W.
Initiate Secure Erase Operation	SANITIZE_START	W/E _P	[165]	0h	
Enable Background Operations	BKOPS_EN	W/E _P	[164]	0h	
Enable Background Operations	BKOPS_EN	R/W	[163]	0h	
Hardware Reset Function	RST_n_FUNCTION	R/W	[162]	0h	
HPI Management	HPI_MGMT	R/W/ E_P	[161]	0h	
Partitioning Support	PARTITIONING_SUPPORT	R	[160]	7h	Can have extended partition attributes; can have enhanced technical features; device supports partitioning.
Maximum Enhanced Area Length	MAX_ENH_SIZE_MULT	R	[159:157]		32GB : 254h 64GB : 4C9h
Partition Attributes	PARTITIONS_ATTR	R/W	[156]	0h	Bit[7:5]: Reserved Bit[4]=1: Set Enhanced attribute in General Purpose partition 4 Bit[3]=1: Set Enhanced attribute in General Purpose partition 3 Bit[2]=1: Set Enhanced attribute in General Purpose partition 2 Bit[1]=1: Set Enhanced attribute in General Purpose partition 1
Partitioning Set Complete	PARTITION_SETTING_COMPLETED	R/W	[155]	0h	

General Purpose Partition Length	GP_SIZE_MULT	R/W	[154:143]	0h	
Enhanced User Data Area Length	ENH_SIZE_MULT	R/W	[142:140]	0h	
Enhanced User Data Start Address	ENH_START_ADDR	R/W	[139:136]	0h	
Reserved	RESERVED	TBD	[135]		
Secure Bad Block Management	SEC_BAD_BLK_MGMT	R/W	[134]	0h	
Production State Awareness	PRODUCTION_STATE_AWARENESS	R/W/E	[133]	0h	
Case Temperature Support	TCASE_SUPPORT	W/E_P	[132]	0h	
Periodic Wakeup	PERIODIC_WAKEUP	R/W/E	[131]	0h	
Support for Programming CID/CSD in DDR Mode	PROGRAM_CID_CSD_DDR_SUPPORT	R	[130]	1h	
Reserved	RESERVED	TBD	[129:128]		
Vendor Specific Field	VENDOR_SPECIFIC_FIELD_FIELD		[127:64]	0h	
Native Sector Size	NATIVE_SECTOR_SIZE	R	[63]	0h	
Use Native Sector	USE_NATIVE_SECTOR	R/W	[62]	0h	
Data Sector Size	DATA_SECTOR_SIZE	R	[61]	0h	
Initialization Timeout (emulation)	INIT_TIMEOUT_EMU	R	[60]	0h	
Class 6 Command Control	CLASS_6_CTRL	R/W/ E_P	[59]	0h	
Dynamic Capacity Needed	DYNCAP_NEEDED	R	[58]	0h	
Exception Events Control	EXCEPTION_EVENTS_CTRL	R/W/ E_P	[57:56]	0h	
Exception Events Status	EXCEPTION_EVENTS_STATUS	R	[55:54]	0h	
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	R/W	[53:52]	0h	
Context Configuration	CONTEXT_CONF	R/W/ E_P	[51:37]	0h	
Packed Command Status	PACKED_COMMAND_STATUS	R	[36]	0h	
Packed Failure Index	PACKED_FAILURE_INDEX	R	[35]	0h	

Power-Off Notification	POWER_OFF_NOTIFICATION	R/W/ E_P	[34]	0h	Host does not support power-off notification; device should not assume any notification.
Cache Control	CACHE_CTRL	R/W/ E_P	[33]	0h	
Cache Flush	FLUSH_CACHE	W/E_ P	[32]	0h	
Control to turn the Barrier ON/OFF	BARRIER_CTRL	R/W	[31]	0h	
Mode Control	MODE_CONFIG	R/W/ E_P	[30]	0h	
Mode Operation Codes	MODE_OPERATION_CODES	W/E_ P	[29]	0h	
Reserved		TBD	[28:27]		
FFU Status	FFU_STATUS	R	[26]	0h	
Pre-loading Data Size	PRE_LOADING_DATA_SIZE	R/W/ E_P	[25:22]	0h	
Max Pre-loading Data Size	MAX_PRE_LOADING_DATA_SIZE	R	[21:18]		64KB : 10000h
64KB : 10000h	PRODUCT_STATE_AWARENESS_ENABLEMENT	R/W/ E & R	[17]	3h	
Secure Removal Type	SECURE_REMOVAL_TYPE	R/W/ E & R	[16]	9h	
Command Queue Mode Enable	CMDQ_MODE_EN	R/W/ E_P	[15]	0h	
Reserved		TBD	[14:0]		