Loongtion®

TECHNICAL WHITEPAPER

Industrial DDR5 SDRAM

Next-generation China domestic DDR5 with 16n prefetch, on-die ECC, and speed grades up to 8400 MT/s, purpose-built for high-bandwidth industrial and embedded systems.

JEDEC Compliant	**Industrial Temp** **−40°C to 85°C**	**16 Gb**

Ningbo Loongtion Intelligent Technology Co., Ltd.
hi@loongtion.com | www.loongtion.com
Document Version 1.1 | June 2026

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1. Executive Summary

This whitepaper presents the Loongtion DDR5 SDRAM, a high-performance, China-domestic memory component designed for industrial, embedded, medical, and commercial applications. Leveraging DDR5 wafers from Hefei ChangXin (CXMT) and packaged and temperature-screened by Ningbo Loongtion Intelligent Technology Co., Ltd. (Loongtion®), this product offers a domestically sourced alternative for systems requiring JEDEC-compliant DDR5 memory.

The Loongtion DDR5 SDRAM supports speed grades from DDR5-3200 through DDR5-8400 for standard configurations, with 3DS-DDR5 variants supporting up to DDR5-6400. Key architectural features include a 16n-bit prefetch architecture, up to 32 banks (x4/x8 configurations), on-die ECC with error scrubbing, a 4-tap decision feedback equalizer (DFE), and comprehensive training and calibration capabilities.

The product is offered in 82-ball WBGA (x4/x8) and 102-ball WBGA (x16) packages, compliant with JEDEC MO-210 standards. Industrial temperature variants are available, including a -40°C to +85°C rated option, making the device suitable for demanding environments.

The Loongtion DDR5 SDRAM is documented in datasheet Rev 1.1 (October 2025), which is currently in a preliminary stage. Note that IDD current values are marked as TBD in the source documentation.

2. Product Overview

2.1 Manufacturer and Supply Chain

The Loongtion DDR5 SDRAM is developed and supplied by **Ningbo Loongtion Intelligent Technology Co., Ltd. (Loongtion®)** . The device uses DDR5 wafers sourced from Hefei ChangXin (CXMT), a leading China-domestic memory manufacturer. Loongtion performs packaging and temperature screening, ensuring suitability for industrial and specific embedded applications.

2.2 Product Type

The Loongtion DDR5 SDRAM is a component-level memory device, available as a packaged DDR5 SDRAM component for integration into memory modules (DIMMs) or direct soldering onto system boards for embedded applications.

2.3 Target Applications

The product is designed for a broad range of applications, including:

- Industrial embedded systems
- Medical devices
- Networking and communications equipment
- Commercial servers and data centers
- China domestic market projects requiring locally sourced memory

2.4 Package Options

Configuration	Package	JEDEC Standard	Ball Count
x4/x8	WBGA	MO-210-AN	82-ball
x16	WBGA	MO-210-AU	102-ball

2.5 Documentation Status

The datasheet for the Loongtion DDR5 SDRAM is currently in a preliminary revision stage:

- **Rev 1.0 (September 2025):** Initial Draft
- **Rev 1.1 (October 2025):** Changed package outline drawing

Certain parameters, including IDD current values, are marked as TBD and are not specified in source documentation.

3. Technology and Architecture

3.1 Core Architecture

The Loongtion DDR5 SDRAM implements the full DDR5 architecture as defined by the JEDEC JESD79-4 standard. Key architectural elements include:

Prefetch Architecture: 16n-bit prefetch — double that of DDR4, enabling higher bandwidth at the same core frequency.

Bank Organization:

Configuration	Bank Groups	Banks per Group	Total Banks
x4/x8	8 (BG0-BG2)	4	32
x16	4 (BG0-BG1)	4	16

The number of banks in a bank group is density-dependent: 8Gb devices use 2 banks per group, while 16Gb devices use 4 banks per group.

Address Configuration:

Parameter	x4	x8	x16
Row Address	R0-R15	R0-R15	R0-R15
Column Address	C0-C10	C0-C9	C0-C9
Page Size	1KB	1KB	2KB

3.2 3DS (3-Dimensional Stacked) Support

The device supports 3DS stacking for x4 configurations, including 2-high (2H) and 4-high (4H) stacks. CID[2:0] is used for logical rank identification, supporting up to 8 logical ranks (CID 0x0-0x7).

3.3 Interface and Signaling

Interface Type: Pseudo Open Drain (POD) interface for data input/output, command, and address input. The device includes internal VREF generation for data input, command and address input, and chip select.

Clock and Strobe Signals:

- Differential clock inputs: CK_t and CK_c
- Bidirectional differential data strobe signals: DQS_t/DQS_c
- The DDR5 SDRAM supports only differential data strobes; single-ended mode is not supported
- For x16 bus: DQSL corresponds to DQL0-DQL7; DQSU corresponds to DQU0-DQU7

3.4 Control Signals

Signal	Function
CS_n	Chip Select; command masking, rank selection, power-down control
CA[13:0]	Command/Address inputs
DM_n, DMU_n, DML_n	Input Data Mask (x8: MR5:OP[5]=1; x4 does not support DM)
TDQS_t, TDQS_c	Termination Data Strobe (x8 only; MR5:OP[4]=1)
RESET_n	Active low asynchronous reset; CMOS rail-to-rail (80%/20% of VDDQ)
ALERT_n	CRC error indicator; connectivity test mode input
TEN	Connectivity test mode enable; CMOS rail-to-rail (80%/20% of VDDQ)
MIR	CA mirror function (VDDQ = swap even/odd CA)
CAI	Command and Address Inversion (VDDQ = invert CA logic levels)
CA_ODT	CA ODT setting selection (VSS = A group; VDDQ = B group)
LBDQ	Loopback Data Output
LBDQS	Loopback Data Strobe (single-ended)
ZQ	Reference pin for ZQ calibration (external 240 Ω resistor to VSS)

3.5 On-Die ECC and Error Protection

The Loongtion DDR5 SDRAM incorporates on-die ECC for error correction, with support for ECC transparency and error scrubbing. This provides enhanced data integrity without requiring external parity or ECC logic from the memory controller.

For data bus integrity, Cyclic Redundancy Check (CRC) is supported for both read and write data paths. When CRC is enabled, the CAS latency value is incremented based on the Read CRC Latency Accumulator.

3.6 Equalization

The device features a 4-tap decision feedback equalizer (DFE) to improve signal integrity at high data rates. The sum of absolute values of Tap-2, Tap-3, and Tap-4 must be less than 60 mV.

3.7 Burst Length Support

The device supports multiple burst length modes:

- BL16
- BC8 OTF (On-The-Fly)

- BL32 (Optional)
- BL32 OTF (Optional)

For fixed BL32 and BL32 OTF modes:

- Read burst length (RBL) = 32 (36 with read CRC enabled)
- Write burst length (WBL) = 32 (36 with write CRC enabled)

3.8 Supported Features

The Loongtion DDR5 SDRAM implements a comprehensive set of features:

- Connectivity test mode (TEN)
- CAI (Command Address Inversion)
- CA Mirror (MIR)
- 1N/2N command mode
- 4-tap decision feedback equalizer (DFE)
- Loopback test and bit error rate test
- hPPR/sPPR; sPPR execute/abort/lock
- Training modes: VrefDQ/VrefCA/VrefCS, Read Training, CA Training, CS Training, Per-Pin VREFDQ, Write Leveling
- Duty Cycle Adjuster (DCA) for Read - Global
- Read Dedicated Per-Pin DCA (Per-Pin DQ)
- Per DRAM Addressability (PDA)
- Maximum Power Saving Mode (MPSM)
- Multi-Purpose Command (MPC)
- Asynchronous reset at power-up
- Auto-refresh and self-refresh modes
- Programmable read and write preamble and postamble
- Read and write CRC
- On-die ECC error correction
- ECC transparency and error scrubbing
- MBIST/mPPR
- Same-bank and all-bank refresh
- Fine-granularity refresh mode (FGR)

3.9 Features Not Supported

- Downshift mode
- Partial Array Self Refresh (PASR)

4. Key Features and Differentiators

4.1 China-Domestic Supply Chain

The Loongtion DDR5 SDRAM uses wafers from CXMT (Hefei ChangXin) and is packaged and tested by Loongtion in China. This provides a domestically sourced DDR5 solution, reducing reliance on foreign memory suppliers and offering improved supply chain security for critical infrastructure projects.

4.2 Wide Operating Temperature Range

The device is available in both standard and industrial temperature variants. Two documented part numbers cover different industrial temperature requirements:

Part Number	Temperature Range
YC5GG16W-9CXDQ-M(0)	-25°C to +85°C
YZ5GG16W-9CXDQ-M(0)	-40°C to +85°C

4.3 Broad Speed Grade Support

The standard device supports speed grades from DDR5-3200 up to DDR5-8400, covering a wide range of system performance requirements. 3DS-DDR5 devices support speeds up to DDR5-6400.

4.4 High Bank Count and Parallelism

With up to 32 banks in x4/x8 configurations, the device offers significant parallelism for improved memory access efficiency and reduced latency under multi-threaded workloads.

4.5 Advanced Signal Integrity Features

The combination of 4-tap DFE, per-pin VREFDQ training, duty cycle adjuster (global and per-pin), CA inversion (CAI), and CA mirror (MIR) provides robust signal integrity at the high data rates required by DDR5 operation.

4.6 Enhanced Reliability

On-die ECC with error scrubbing, CRC on both read and write data paths, hPPR/sPPR, and MBIST support contribute to high system reliability. This makes the device suitable for mission-critical applications in industrial and medical environments.

4.7 Comprehensive Training and Calibration

The device supports all JEDEC-required training modes for robust system bring-up, including VrefDQ, VrefCA, VrefCS, Read Training, CA Training, CS Training, per-pin VREFDQ, and Write Leveling. ZQ calibration is supported using an external 240 Ω resistor.

5. Technical Specifications

5.1 Electrical Specifications: Supply Voltages

Parameter	Nominal	Min	Max	Tolerance
VDD/VDDQ	1.1 V	1.067 V	1.166 V	-3%/+6%

VPP	1.8 V	1.71 V	1.89 V	±5%

Voltage Constraints:

- The voltage difference between VDD and VDDQ must always be kept within 300 mV
- VPP voltage must always be equal to or greater than the maximum of VDD and VDDQ
- AC parameters are measured with VDD and VDDQ shorted together

5.2 Absolute Maximum Ratings

Parameter	Min	Max
VDD and VDDQ relative to VSS	-0.3 V	1.4 V
VPP relative to VSS	-0.3 V	2.1 V
Any pin voltage relative to VSS	-0.3 V	1.4 V

5.3 Impedance Specification (Z(f))

Frequency Range	Maximum Impedance
DC to 2 MHz	10 mOhm
20 MHz	20 mOhm

Applies to VDD, VDDQ, and VPP domains for all pins within each voltage domain. Does not include the DRAM package and silicon die.

5.4 Operating Temperature Ranges

Range	Symbol	Temperature	Notes
Normal	Toper_normal (NT)	0°C to 85°C	Per JESD402-1
Extended	Toper_extended (XT)	85°C to 95°C	Host must provide extended refresh control
Industrial	—	-25°C to +85°C	Part number YC5GG16W-9CXDQ-M(0)
Industrial	—	-40°C to +85°C	Part number YZ5GG16W-9CXDQ-M(0)
Storage	TSTG	-55°C to +100°C	Absolute maximum rating

Operating temperature refers to DRAM center/top case surface temperature per JESD51-2. For 3DS devices, derate temperature by 2.5°C × $\log_2(N)$, where N = number of stacked die.

5.5 Package Options

Configuration	Package	JEDEC Standard
x4/x8	82-ball WBGA	MO-210-AN
x16	102-ball WBGA	MO-210-AU

Support balls in both packages are for mechanical support only and should not be connected to high or low logic levels.

5.6 Speed Grade Timing Parameters (Primary Grades)

Speed Grade	CL-nRCD-nRP	tCK(min)	CAS Latency
DDR5-4800	40-39-39	0.416 ns	40 nCK
DDR5-5600	46-45-45	0.357 ns	46 nCK
DDR5-6400	52-52-52	0.313 ns	52 nCK

5.7 Supported Speed Grades

All supported speed grades: DDR5-3200, DDR5-3600, DDR5-4000, DDR5-4400, DDR5-4800, DDR5-5200, DDR5-5600, DDR5-6000, DDR5-6400, DDR5-6800, DDR5-7200, DDR5-7600, DDR5-8000, DDR5-8400.

3DS-DDR5 supported speed grades: DDR5-3200 to DDR5-6400 (x4 2H & 4H).

5.8 Clock Period (tCK(avg) minimum)

Speed Grade	tCK(avg)min
DDR5-3200	0.625 ns
DDR5-3600	0.555 ns
DDR5-4000	0.500 ns
DDR5-4400	0.454 ns
DDR5-4800	0.416 ns
DDR5-5200	0.384 ns
DDR5-5600	0.357 ns
DDR5-6000	0.333 ns
DDR5-6400	0.312 ns

tCK(avg)max is defined as 1.010 ns (1980 MT/s data rate) to meet 1% SSC downward spread requirement at 2000 MT/s per JESD79-4.

5.9 Supported CAS Latencies

Speed Grade	Supported CL Values (nCK)
DDR5-4800	22, 26, 28, 30, 32, 36, 40, 42
DDR5-5600	22, 26, 28, 30, 32, 36, 40, 42, 46, 50
DDR5-6400	22, 26, 28, 30, 32, 36, 40, 42, 46, 50, 52, 54, 56

The device supports only even CAS latencies; odd CAS latencies are rounded up to the nearest even value. The 1980–2100 MT/s data rate always uses CL22.

5.10 Key Timing Parameters (All Speed Grades)

Parameter	Description	Min	Max
tAA	Read command to first data	16.000 ns	22.222 ns
tRCD	Row to column delay	16.000 ns	—
tRP	Row Precharge Time	16.000 ns	—
tRAS	Active to Precharge	32.000 ns	5×tREFI (std) / 9×tREFI (FGR)
tRC	ACT to ACT/REF	48.000 ns	—
tWR	Write recovery time	30.000 ns	—

CAS Write Latency (CWL) = CL - 2.

5.11 Command Delays

Parameter	Description	Value
tCCD_L	Read-to-Read, same bank group	max(8nCK, 5ns)
tCCD_L_WR	Write-to-Write, same bank group	max(32nCK, 20ns)
tCCD_L_WR2	Write-to-Write, same bank group, no RMW	max(16nCK, 10ns)
tCCD_S	Read-to-Read, different bank groups	8 nCK
tCCD_S_WR	Write-to-Write, different bank groups	8 nCK
tRRD_L	ACT-to-ACT, same bank group	max(8nCK, 5ns)
tRRD_S	ACT-to-ACT, different bank groups	8 nCK
tRTP	Read to Precharge	max(12nCK, 7.5ns)
tPPD	Precharge to Precharge	2 nCK
tCCD_L_WTR	Write-to-Read, same bank group	CWL + WBL/2 + max(16nCK, 10ns)
tCCD_S_WTR	Write-to-Read, different bank groups	CWL + WBL/2 + max(4nCK, 2.5ns)

5.12 Refresh Timing

Condition	tREFI	Refresh Cycle
0°C ≤ TCASE ≤ 85°C (Normal)	3.9 µs	8K cycles / 32 ms
85°C < TCASE ≤ 95°C (Normal)	1.95 µs	8K cycles / 16 ms
0°C ≤ TCASE ≤ 85°C (FGR 2x)	1.95 µs	—
85°C < TCASE ≤ 95°C (FGR 4x)	0.975 µs	—

5.13 Output Driver Impedance (RON)

Setting	Nominal	Range
34Ω pull-down (RON34Pd) at 0.5×VDDQ	1.0 × RZQ/7	0.8–1.1 RZQ/7
34Ω pull-down (RON34Pd) at 0.8×VDDQ	1.0 × RZQ/7	0.9–1.1 RZQ/7
34Ω pull-down (RON34Pd) at 0.95×VDDQ	1.0 × RZQ/7	0.9–1.25 RZQ/7
34Ω pull-up (RON34Pu) at 0.5×VDDQ	1.0 × RZQ/7	0.9–1.25 RZQ/7
34Ω pull-up (RON34Pu) at 0.8×VDDQ	1.0 × RZQ/7	0.9–1.1 RZQ/7
34Ω pull-up (RON34Pu) at 0.95×VDDQ	1.0 × RZQ/7	0.8–1.1 RZQ/7
48Ω pull-down (RON48Pd)	1.0 × RZQ/5	0.8–1.25 RZQ/7
48Ω pull-up (RON48Pu)	1.0 × RZQ/5	0.8–1.25 RZQ/7

RZQ = 240 Ω for output driver calibration.

5.14 IDD Current Types

The following IDD current types are defined for the Loongtion DDR5 SDRAM:

IDD0, IDDQ0, IPP0, IDD0F, IDDQ0F, IPP0F, IDD2N, IDDQ2N, IPP2N, IDD2NT, IDDQ2NT, IPP2NT, IDD2P, IDDQ2P, IPP2P, IDD3N, IDDQ3N, IPP3N, IDD3P, IDDQ3P, IPP3P, IDD4R, IDDQ4R, IPP4R, IDD4RC, IDD4W, IDDQ4W, IPP4W, IDD4WC, IDD5F, IDDQ5F, IPP5F, IDD5B, IDDQ5B, IPP5B, IDD5C, IDDQ5C, IPP5C, IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD7, IDDQ7, IPP7, IDD8, IDDQ8, IPP8, IDD9, IDDQ9, IPP9

Note: IDD current values are not specified in source documentation (marked TBD).

5.15 Capacitance and ESD

Not specified in source documentation (referenced in Tables 8-1 through 8-4 of the datasheet; values not extracted).

5.16 Clock Jitter Parameters

Parameter	DDR5-4800	DDR5-5600	DDR5-6400
Duty cycle error (tCK_duty_cycle_UI_error)	max 0.05 UI	max 0.05 UI	TBD
Rj RMS (1-UI, no BUJ)	max 0.0037 UI	max 0.0037 UI	TBD
Dj p-p (1-UI, no jitter)	max 0.030 UI	max 0.030 UI	TBD
Tj (1-UI, no BUJ)	max 0.090 UI	max 0.090 UI	TBD
Rj RMS (N-UI, N=2,3, no BUJ)	max 0.0040 UI	max 0.0040 UI	TBD
Dj p-p (N-UI, N=2,3, no BUJ)	max 0.074 UI	max 0.074 UI	TBD
Tj (N-UI, N=2,3, no BUJ)	max 0.140 UI	max 0.140 UI	TBD

5.17 Differential Input Clock Parameters

Parameter	Value
VIX_CK_Ratio (crossover voltage ratio)	max 50%
VIHdiffCK	0.75 × Vdiffpp
VILdiffCK	0.25 × Vdiffpp
SRdiff_CK (DDR5-4800)	2–14 V/ns
SRdiff_CK (DDR5-5600/6400)	2–30 V/ns

5.18 DQ Timing Margin Parameters

Parameter	DDR5-4800	DDR5-5600	DDR5-6400
tRx_DQ_tMargin	min 0.825 UI	min 0.835 UI	min 0.845 UI
ΔtRx_DQ_tMargin_DQS_DCD	max 0.06 UI	max 0.06 UI	max 0.06 UI
ΔtRx_DQ_tMargin_DQS_Rj	max 0.09 UI	max 0.09 UI	max 0.09 UI
ΔtRx_DQ_tMargin_DQS_DCD_Rj	max 0.15 UI	max 0.15 UI	max 0.15 UI
tRx_DQS2DQ	114–729 ps	114–714 ps	114–703 ps
tRx_DQ2DQ	max 50 ps	max 50 ps	max 50 ps

6. Performance and Reliability

6.1 Timing Algorithm and Precision

Timing parameters are defined based on nominal tCK(avg)min for DDR5-3200 to DDR5-5200, and on nominal tCK(avg)min for DDR5-5600 to DDR5-6400. Minimum timing parameter values are rounded down and defined with 1 ps precision. A correction factor of 99.70% (0.30% reduction) is applied for minimum timing parameters. Integer-only floor math rounding algorithm takes precedence in case of conflicting results.

6.2 BER (Bit Error Rate) Requirements

The Loongtion DDR5 SDRAM specifies a minimum BER of 1×10^{-16} at the receiver slicer (after equalization) for stressed eye conditions. The eye is verified by measuring to a BER of 1×10^{-9} and extrapolating to 1×10^{-16}. A minimum BER requirement of E-9 per pin with 99.5% confidence level is specified.

6.3 Output Slew Rates

Parameter	**DDR5-4800**	**DDR5-5600**	**DDR5-6400**
Single-ended output slew rate (SRQse)	—	12–24 V/ns	—
Differential output slew rate (SRQdiff)	16–48 V/ns	24–48 V/ns	24–48 V/ns

Note: Output slew rates are verified by design and characterization, not subject to production test.

6.4 Stressed Eye Parameters (Golden Reference Lane 1)

Parameter	**DDR5-4800**	**DDR5-5600**	**DDR5-6400**
RxEH_StressedEye	max 70 mV	max 60 mV	max 57.5 mV
RxEW_StressedEye	max 0.25 UI	max 0.235 UI	max 0.230 UI
Vswing_StressedEye	max 600 mV	max 600 mV	max 600 mV
Sj_StressedEye (200 MHz)	max 0.45 UI p-p	max 0.45 UI p-p	max 0.45 UI p-p
Rj_StressedEye (10 MHz–1 GHz)	0–0.04 UI RMS	0–0.04 UI RMS	0–0.04 UI RMS
Vnoise_StressedEye (PRBS23)	0–125 mV pk-pk	0–125 mV pk-pk	0–125 mV pk-pk

6.5 Loopback Timing (4-way interleave)

Parameter	**DDR5-4800/5600**	**DDR5-6400**
tLBQSL (LBDQS low-level time)	min 0.7 tCK	min 0.75 tCK
tLBQSH (LBDQS high-level time)	min 0.7 tCK	min 0.75 tCK
tLBDQSQ (LBDQS to LBDQ skew)	max 0.5 tCK/2	max 0.5 tCK/2
tLBQH (LBDQ hold time)	min 0.5 tCK/2	min 0.5 tCK/2
tLBDVW (Data valid window per subchannel)	1.6–2 tCK/2	1.6–2 tCK/2

6.6 Reliability Features

The device incorporates multiple features to enhance system reliability:

- **On-die ECC:** Corrects single-bit errors; supports transparency and error scrubbing for ongoing data integrity.
- **CRC:** Cyclic Redundancy Check on both read and write data paths for data bus integrity.
- **hPPR/sPPR:** Hard and Soft Post-Package Repair for memory cell repair after assembly.
- **MBIST:** Memory Built-In Self-Test for manufacturing and diagnostic testing.
- **Error Scrubbing:** Active detection and correction of accumulated errors.
- **MPSM:** Maximum Power Saving Mode for reduced power consumption.

6.7 Lower Frequency Operation

The Loongtion DDR5 SDRAM supports functional operation at frequencies lower than its rated speed grade. This is design/characterization verified but not production test qualified per JEDEC standard.

7. Applications and Target Markets

7.1 Industrial Embedded Systems

The Loongtion DDR5 SDRAM is well-suited for industrial PCs, PLCs (Programmable Logic Controllers), edge gateways, and factory automation equipment. The wide temperature range options (-25°C to +85°C and -40°C to +85°C) and robust reliability features make it appropriate for demanding industrial environments where temperature extremes and long-term reliability are critical.

7.2 Medical Devices

Medical imaging systems, patient monitoring equipment, and diagnostic devices require high reliability and consistent performance. The on-die ECC, CRC support, and JEDEC compliance of the Loongtion DDR5 SDRAM make it a suitable choice for medical applications where data integrity is paramount.

7.3 Networking and Communications

Routers, switches, 5G base stations, and other networking infrastructure require high-bandwidth memory with excellent signal integrity. The DDR5 architecture, 4-tap DFE, and comprehensive training capabilities of the Loongtion DDR5 SDRAM support the data rates and signal quality needed for these applications.

7.4 Commercial Servers and Data Centers

As a component for DDR5 DIMMs, the Loongtion DDR5 SDRAM can be used in cloud computing, enterprise servers, and data center applications requiring high memory bandwidth and capacity.

7.5 Automotive and Transportation

The -40°C to +85°C temperature range of the YZ5GG16W part number makes the device suitable for automotive infotainment, telematics, and certain ADAS (Advanced Driver-Assistance Systems) applications that operate within this temperature envelope.

7.6 China Domestic Market

The Loongtion DDR5 SDRAM is primarily targeted at the China domestic market, including government, defense, and critical infrastructure projects that require locally sourced memory solutions. The use of CXMT wafers and domestic packaging provides supply chain security and regulatory compliance.

8. System Integration and Design Considerations

8.1 Power Supply Sequencing

The following constraints must be observed during power-up, normal operation, and power-down:

- The voltage difference between VDD and VDDQ must always be kept within 300 mV
- VPP voltage must always be equal to or greater than the maximum of VDD and VDDQ

8.2 Reset and Initialization

- RESET_n must be HIGH during normal operation
- After RESET_n is driven low, voltage must remain below VIL(DC)_RESET during tPW_RESET (minimum 1.0 ns pulse width)
- Once RESET_n is driven high, voltage must be maintained above VIH(DC)_RESET
- Reset operation results in loss of data contents — a full initialization sequence must be executed after reset
- In connectivity test mode (TEN), no refresh operations occur; upon exiting CT mode, the device state is unknown and a reset initialization sequence must be executed

8.3 Pin Connection Guidelines

Pin	**Recommendation if Unused**
ALERT_n	Tie to VDDQ
MIR	Tie to VSS if CA mirror function not needed
CAI	Connect to VSS if CA inversion not required
CA[13]	Connect ball to VDDQ regardless of MIR status
ZQ	Requires external 240 Ω resistor (RZQ) to VSS

Support balls in both package options (82-ball and 102-ball) are for mechanical support only and should not be connected to high or low logic levels.

8.4 Output Loading and Timing

AC timing and output slew rate are defined using a 50-ohm effective reference load. The reference level for output signals is 0.7 × VDDQ. System designers should use IBIS or other simulation tools to correlate the timing reference load with the system environment.

8.5 Calibration Recommendations

Output driver impedance calibration is recommended at 0.8 × VDDQ. Alternative calibration schemes may be used (e.g., 0.5 × VDDQ and 0.95 × VDDQ). Tolerance limits are specified after calibration under stable voltage and temperature. Behavior after voltage/temperature changes is not specified in source documentation.

8.6 Test Conditions

- Spread spectrum clocking (SSC) must be disabled during jitter and eye testing
- Continuous clock mode output is enabled by setting MR25 OP[3] to "1"
- Test pattern for eye parameters: continuous PRBS8 LFSR training pattern through all DQ channels
- Tested on CTC2 card only

8.7 3DS Temperature Derating

For 3DS stacked devices, the operating temperature must be derated by 2.5°C × $\log_2(N)$, where N = number of stacked die.

8.8 Lower Frequency Operation

When the DRAM operates at a data rate lower than 4800 MT/s, DDR5-4800 AC timing parameters apply. Any speed bin supports functional operation at lower frequencies (design/characterization verified, not production test qualified).

9. Standards Compliance and Quality

9.1 JEDEC Compliance

The Loongtion DDR5 SDRAM is compliant with the following JEDEC standards:

Standard	Description
JESD79-4	DDR5 SDRAM Specification (including SSC downward spread requirement)
JESD402-1	Temperature range definition (normal and extended)
JESD51-2	Case temperature measurement methodology

9.2 Environmental Compliance

The device is stated as RoHS compliant.

9.3 Package Standards

Configuration	JEDEC Standard
x4/x8 (82-ball WBGA)	MO-210-AN
x16 (102-ball WBGA)	MO-210-AU

9.4 Quality Documentation

The product is documented in a 12-part datasheet structure. Current revision history:

- Rev 1.0 (September 2025): Initial Draft
- Rev 1.1 (October 2025): Changed package outline drawing

9.5 Known Documentation Notes

The following notes are documented from the source material for transparency:

- **DM_n function description:** One section states "The device does not support the DM function" immediately after describing DM_n operation for x8 devices. This may be a documentation error or refer to a specific device variant.
- **VRx_CK for DDR5-6400:** Listed as 100 mV with a parenthetical note "*120" — conflicting values.
- **IDD current values:** All marked as TBD in source documentation.

9.6 Design Verification vs. Production Test

Output slew rates are verified by design and characterization and are not subject to production test.

10. Ordering Information

The following part numbers are documented in the source material:

Part Number	Density	Organization	Package	Temperature Range
YC5GG16W-9CXDQ-M(0)	16 Gb	2 Gb × 8	WBGA-82	-25°C to +85°C
YZ5GG16W-9CXDQ-M(0)	16 Gb	2 Gb × 8	WBGA-82	-40°C to +85°C

Note: Additional densities, organizations, speed grades, and package configurations may be available. Contact Loongtion for complete ordering information and the full product portfolio.

11. About Loongtion

Ningbo Loongtion Intelligent Technology Co., Ltd. (Loongtion®) is a China-domestic developer and supplier of memory and solid-state storage products. The company's product portfolio includes:

- **Memory Products:** DDR3, DDR4, DDR5, and LPDDR4X SDRAM components
- **Storage Products:** eMMC 5.1, M.2 NVMe SSD, and NVMe BGA SSD solutions

Loongtion serves the industrial, embedded, medical, and commercial markets, offering China-domestic sourcing through CXMT wafer partnerships and local packaging and testing capabilities. This vertically integrated approach provides customers with supply chain security, reduced lead times, and locally supported product lifecycles.

Contact Information:

- **Email:** hi@loongtion.com
- **Website:** www.loongtion.com

Disclaimer: Specifications may change without notice. Users should refer to the latest official datasheet from Ningbo Loongtion Intelligent Technology Co., Ltd. (www.loongtion.com) for current and complete technical information. The technical facts presented in this whitepaper are based solely on provided source documentation (Rev 1.1, October 2025). Certain values, including IDD current parameters, are not specified in the source and are marked accordingly.