



DDR3 SDRAM Data Sheet

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Revision History

Revision	Date	Description
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Rev 1.1	2022/06	Official Release
Rev 1.2	2022/07	Added normal operating temperature
Rev 1.3	2024/11	Added junction temperature and thermal resistance parameters
Rev 1.4	2025/09	Modified pinout diagram and pin signal descriptions
Rev 2.0	2026/01	Deleted Table 50 'Automotive-Grade' extended temperature
Rev 2.1	2026/4	Added address pin A15 for 8Gb
Rev 2.2	2026/5	Changed RQZ to RZQ in Table 69 and Table 70, and corrected unit description to Ω

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1. Introduction

All control and address inputs are synchronized with a pair of external differential clocks. Inputs are sampled at the crossing point of the differential clock (rising edge of CK and falling edge of CK#). All I/Os are synchronized in a source-synchronous manner with a single-ended DQS signal or a differential DQS pair.

The device operates with a supply voltage of 1.5 V $\pm$ 0.075 V or 1.35 V (-0.067 V / +0.1 V).

The package type is BGA.

2. Product List

Table 1 Product Package Information

Capacity	Organization	Package	Part Number	Operating Temperature
2Gb	128Mb $\times$ 16	96-ball FBGA	YZ38E16SBB-9MFB-M(0)	-40°C ~ 85°C
			YZ38E16SBB-9MFB-M	-55°C ~ 105°C
4Gb	256Mb $\times$ 16	96-ball FBGA	YZ38F16SBB-9MFD-M(0)	-40°C ~ 85°C
			YZ38F16SBB-9MFD-M	-55°C ~ 105°C
8Gb	512Mb $\times$ 16	96-ball FBGA	YZ38G16SDB-9INN-M(0)	-40°C ~ 85°C

3. Product Features

- VDD = VDDQ = 1.5V(1.45V ~ 1.575V);
VDD = VDDQ = 1.35 V (1.28 V to 1.45 V), backward compatible with 1.5 V
- 8 banks;
- 8n-bit prefetch DDR architecture;
- Differential clock (CK, CK#) control;
- Bidirectional differential data strobe (DQS, DQS#);
- On-chip PLL ensures alignment of CK with DQ, DQS, and DQS#;
- DM mask writes data on both rising and falling edges of data strobe.
- All address and control input signals, except data, data strobe, and data mask, are latched on the rising edge of the clock.
- Supports programmable CAS latency of 5, 6, 7, 8, 9, 10, 11, 12, 13, 14.
- Supports programmable additive latency (AL) of 0, CL-1, CL-2.
- Programmable CAS write latency (CWL) = 5, 6, 7, 8, 9, 10.
- Programmable burst length (BL) of 4 or 8, supporting sequential and interleaved modes.
- Burst length (BL) can be changed on-the-fly.
- Output driver strength selected via MRS.
- Supports dynamic on-die termination (ODT).
- Supports asynchronous RESET#.
- Self-calibration: internal calibration via ZQ pin (RZQ = 240 Ω $\pm$ 1%).
- Supports write leveling.
- Supports Temperature-Controlled Self-Refresh (SRT);
- Supports Automatic Self-Refresh (ASR);

- JEDEC Standard Package: 96-ball FBGA (×16);×
- Lead-Free, RoHS Compliant;
- JEDEC Standard;
- Operating temperature: Industrial grade -I (-40°C to 85°C)

Table 2 Product Memory Parameters

Speed	800	1066	1333	1600	1866	2133	Unit
	6-6-6	7-7-7	9-9-9	11-11-11	13-13-13	14-14-14	
tCK(min)	2.5	1.875	1.5	1.25	1.071	0.938	ns
CAS Latency	6	7	9	11	13	14	nCK
tRCD(min)	15	13.125	13.5	13.75	13.91	13.09	ns
tRP(min)	15	13.125	13.5	13.75	13.91	13.09	ns
tRAS(min)	37.5	37.5	36	35	34	33	ns
tRC(min)	52.5	50.625	49.5	48.75	47.91	46.09	ns

Note: The functions and timing specifications described in this datasheet apply to DLL on mode.

Physical Characteristics

- 96-ball FBGA (×16) package;
- Physical dimensions: 9 mm × 13.0 mm × 1.2 mm;

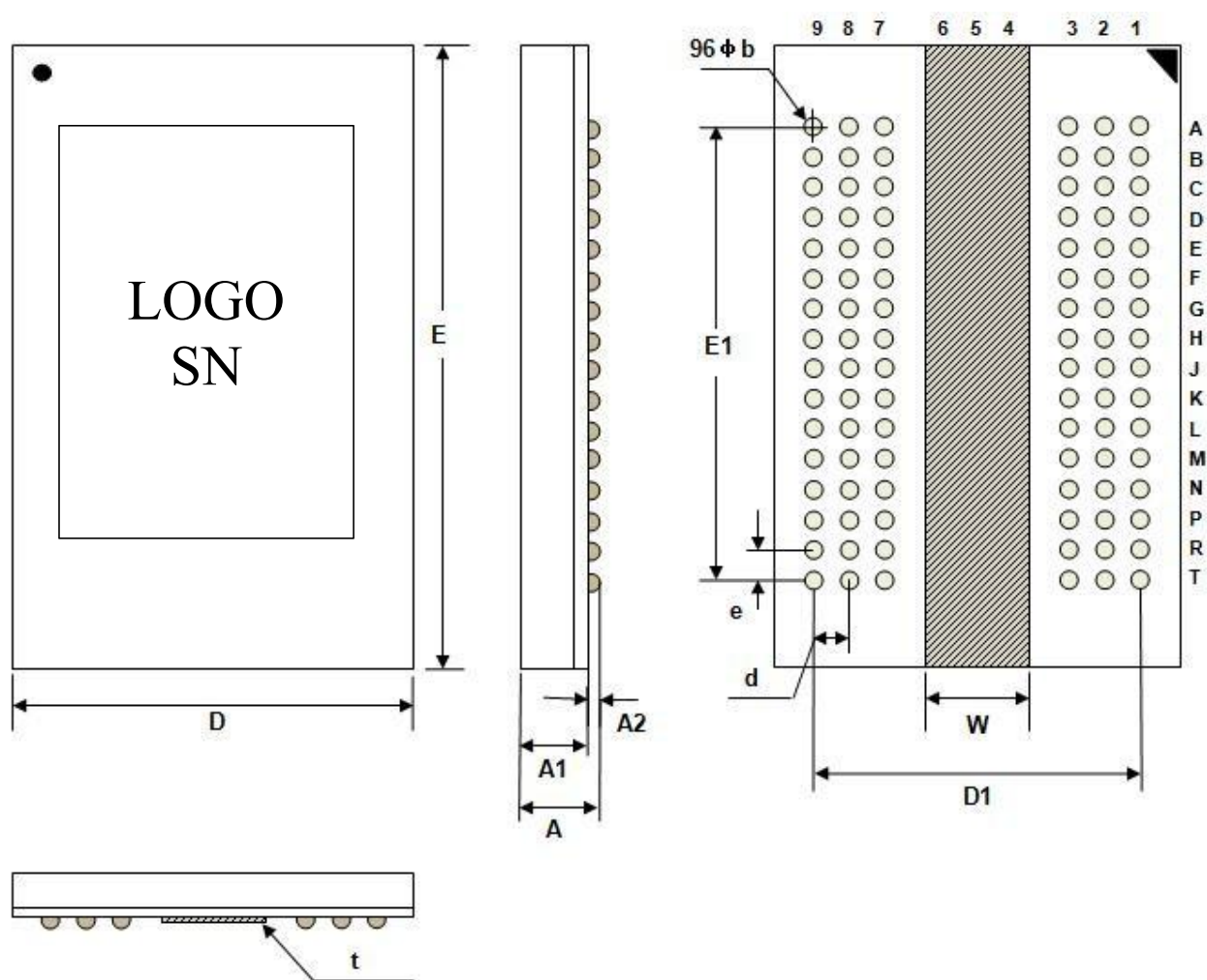


Figure 1 Physical Dimensions Diagram

Table 3 Product Dimension Information

Dimension Symbol	Major Dimension (mm)			Dimension Symbol	Major Dimension (mm)		
	Min	Nom	Max		Min	Nom	Max
A	-	1.12	1.20	W	-	-	2.00
A1	0.73	0.78	0.83	t	0.10	0.15	0.20
A2	0.30	0.35	0.40	e	-	0.80	-
D	8.90	9.00	9.10	D1	6.30	6.40	6.50
E	12.90	13.00	13.10	E1	11.90	12.00	12.10
d	-	0.80	-	b	0.40	0.45	0.50

● Pin Definition

The pin diagram is shown below in Top View:

	1	2	3	4	5	6	7	8	9	
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	A
B	VSSQ	VDD	VSS				DQSU#	DQU6	VSSQ	B
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	C
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	D
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ	E
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ	F
G	VSSQ	DQL6	DQSL#				VDD	VSS	VSSQ	G
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	H
J	NC	VSS	RAS#				CK	VSS	NC	J
K	ODT	VDD	CAS#				CK#	VDD	CKE	K
L	NC	CS#	WE#				A10/AP	ZQ	NC	L
M	VSS	BA0	BA2				A15/NC	VREFCA	VSS	M
N	VDD	A3	A0				A12/BC#	BA1	VDD	N
P	VSS	A5	A2				A1	A4	VSS	P
R	VDD	A7	A9				A11	A6	VDD	R
T	VSS	RESET#	A13				A14	A8	VSS	T
	1	2	3	4	5	6	7	8	9	

Figure 2 Pin Assignment Diagram

● Pin Signal Descriptions

Table 4 Pin Signal Descriptions

96-Ball Device	Symbol	Type	Ball Function
J7, K7	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All control and address input signals are sampled at the crossing of the rising edge of CK and the falling edge of CK#.
K9	CKE	Input	Clock Enable: CKE enables (HIGH) or disables the internal clock signal, input buffers, and output drivers. When CKE is LOW, it provides precharge power-down and self-refresh operation (all banks idle) or active power-down (row active in any bank). o CKE is synchronous for power-down entry/exit and self-refresh entry, and asynchronous for self-refresh exit. After VREF becomes stable during power-up and initialization, VREF must remain stable for the CKE receiver to operate properly. VREF must be maintained for correct self-refresh operation. CKE must be HIGH during read and write accesses. Input buffers (except CK, CK#, CKE, RESET#, and ODT) Disabled during power-down. Input buffers (except CKE) are disabled during self-refresh.
L2	CS#	Input	Chip Select: When CS# is high, all commands are masked. o CS# provides on-chip selection for multiple memory ranks, and CS# is part of the command code.
J3, K3, L3	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, WE#, together with CS#, define a command.
D3, E7	DMU, DML	Input	Data Mask: DM is the input mask signal for write data. During a write, when the DM signal accompanying the input data is sampled high, the input data is masked. The DM signal is sampled on both the rising and falling edges of DQS. For x8 mode, when A11 of mode register MR1 is set, X DM is enabled as TDQS function.
M2,N8,M3	BA0,BA1,BA2	Input	Bank address inputs: BA0, BA1, BA2 are used to select a specific bank. Used to select a specific bank and execute read, write, or precharge commands. During MRS cycles, BA0, BA1, BA2 determine the loading of the corresponding mode register.
L7	A10/AP	Input	Auto Precharge: A10 is sampled during read/write commands to determine whether auto precharge should be performed on the accessed bank after the read/write operation. (HIGH: auto precharge; LOW: no auto precharge.) During a precharge command, A10 is sampled to determine whether precharge is applied to one bank (A10 LOW) or all banks (A10 HIGH). If only a single bank is targeted, that bank is selected by the bank address.
N3,P7 ,P3, N2 ,P8,P2,R8,R2 , T8 , R3 , R7 , N7,T3,T7	A0,A1,A2,A3,A4,A5,A6,A7 ,A8,A9,A10,A11,A12 ,A13,A14,A15	Input	Address Input: Provides the row address for activate commands and the column address for read/write commands. /write commands to select a location in the appropriate bank's memory array. Address inputs provide the op-code during Mode Register Set commands. (op-code).

N7	BC#	Input	Burst Terminate: The BC# signal is sampled during read/write commands to determine whether a burst terminate operation (on-the-fly mode) will be performed. (HIGH: perform burst terminate; LOW: do not perform burst terminate.) HIGH: perform burst terminate; LOW: do not perform burst terminate.
K1	ODT	Input	On-Die Termination Enable: ODT HIGH enables termination resistors inside DDR3. When enabled, ODT resistance is applied to each $\times$ DQ, DQS, DQS#, DM, TDQS, TDQS#, NU pins
			on the pins. (TDQS is enabled by configuring MR1 bit A11 = 1). Enabled. If MR1 and MR2 are programmed to disable RTT, then the ODT pin will be ignored.
T2	RESET#	Input	Active-low reset signal: The reset function is active when RESET# is LOW and inactive when HIGH. During normal operation, RESET# must be held HIGH. RESET# is a CMOS rail-to-rail signal. VOH = 80% of VDD, VOL = 20% of VDD. For example: VDD is HIGH, VSS is LOW.
E3,F7,F2,F8, H3,H8,G2,H7 , D7, C3,C8, C2,A7,A2,B8 ,A3	DQL0,DQL1,DQL2, DQL3,DQL4,DQL5, DQL6,DQL7,DQU0, DQU1,DQU2,DQU3, DQU4,DQU5,DQU6, DQU7	I/O	Data Input/Output: Bidirectional data bus
F3,G3, C7,B7	DQSL , DQSL# , DQSU,DQSU#	I/O	Data strobe: output for read data, input for write data. Read data is edge-aligned, write data is center-aligned. DDR3 supports only differential data strobe, not single-ended data strobe.
J1,L9,M7,J9, L1	NC	-	No connect: These pins should be left floating (the pins are not connected to the DRAM or other pins). the DRAM or other pins).
A1,C1,F1,H2 , A8 , C9 , E9 , H9	VDDQ	Power supply	DQ Supply: 1.35V (-0.067V/+0.1V) 1.5V $\pm$ 0.075V $\pm$
N1,R1,B2,K2 ,G7,K8,D9, N9,R9	VDD	Power supply	Supply: 1.35V (-0.067V/+0.1V) 1.5V $\pm$ 0.075V
B1,D1,G1,E2 , D8 , E8 , B9 , F9,G9,	VSSQ	Power supply	DQ Supply Ground
E1,M1,P1,T1 ,J2,B3,G8,J8 ,A9,M9,P9, T9	VSS	Power supply	Ground
H1	VREFDQ	Power supply	Reference voltage for DQ.
M8	VREFCA	Power supply	Reference voltage for control, command, and address.

L8	ZQ	Power supply	External reference for output driver calibration.
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Note: Only input pins (BA0-BA2, A0-A14, RAS#, CAS#, WE#, CS#, CKE, ODT, RESET#) do not provide termination.

Electrical Characteristics

- Operating Voltage Range:

VDD = VDDQ = 1.5V(1.45V ~ 1.575V);

VDD = VDDQ = 1.35V (1.28V ~ 1.45V), backward compatible with 1.5V.

- Ambient Temperature: Industrial:

Operating Temperature (Tc): -40°C to 85°C; Storage Temperature (Tstg): -

55°C to 110°C. Wide Temperature Range:

Operating Temperature (Tc): -55°C to 105°C; Storage Temperature (Tstg): -55°C to 110°C.

- Absolute Maximum Ratings:

Junction Temperature: Tj

max: 125°C; Thermal

Resistance: 28.3°C/W.

- ROHS

RoHS compliant.

4. State Diagram

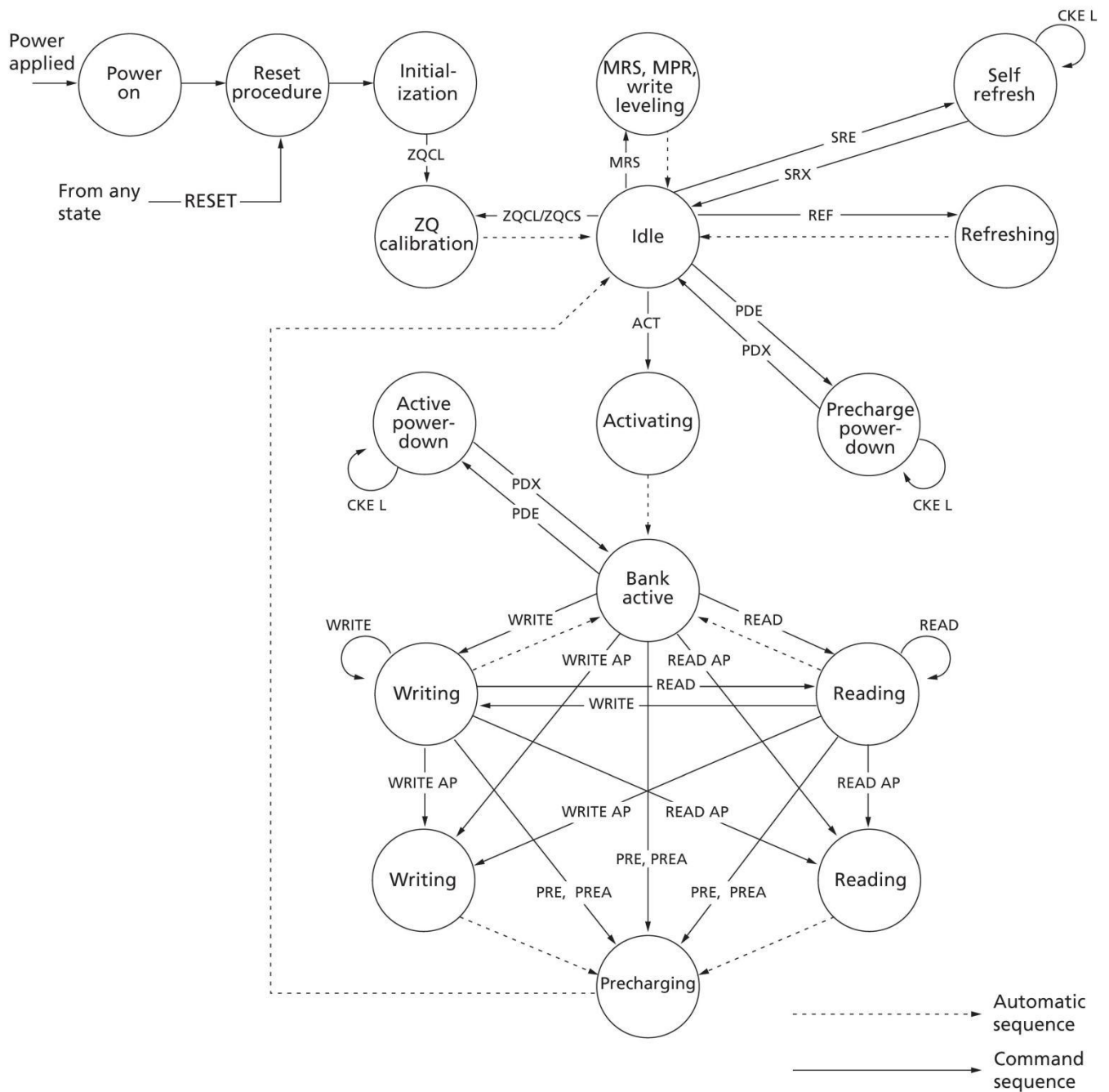


Figure 3 Chip Functional Block Diagram

Table 5 State Diagram Command Definitions

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	Read	RD, RDS4, RDS8	PED	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self Refresh Entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8	SRX	Self Refresh Exit
REF	Refresh	RESET#	RESET Procedure	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	ZQCS	ZQ Calibration Short	-	-

5. Basic Functions

DDR3 SDRAM B-Die component is a high-speed dynamic random-access memory with 8 banks of DRAM. The DDR3 SDRAM uses an 8n prefetch architecture to achieve high-speed operation. This architecture is combined with an interface that enables the I/O pins to transfer two words per clock cycle. A single read or write operation for the DDR3 SDRAM consists of an 8n-byte-wide data block, with data transferred in 4 clock cycles in the DRAM core and 4 clock cycles at the I/O pins, completing the transfer of the corresponding n-byte width.

Read and write operations of the DDR3 SDRAM are burst-oriented, starting at a selected location and continuing for a programmed BL8 or BC4 sequence. Operation begins with the registration of an ACTIVATE command, followed by a READ or WRITE command. Address bits registered with the ACTIVATE command are used to select the bank and row address. Address bits registered with the READ or WRITE command are used to select the starting column location for the burst operation, determine whether auto precharge is performed (via A10), and, if enabled in the mode register, select BC4 or BL8 mode on-the-fly (via A12).

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information on device reset and initialization, register definitions, command descriptions, and device operation.

Reset and Initialization

Power-Up Initialization Procedure

Power-up and initialization require the following sequence:

1. Apply power (it is recommended to keep RESET# below $0.2 \times VDD$; all other inputs may be undefined). RESET# must be held for at least 200 μ s after the power supply is stable. Prior to RESET# de-assertion (minimum 10 ns), CKE is driven LOW. The power supply ramp time between 300 mV and minimum VDD must be within 200 ms; and during the ramp, $VDD > VDDQ$ and $(VDD - VDDQ) < 0.3$ V.
 - VDD and VDDQ are driven by a single power supply.
 - Voltage levels on all pins except VDD, VDDQ, VSS, and VSSQ must be less than or equal to VDD and VDDQ, and must be greater than or equal to VSS and VSSQ. In addition, after power supply voltage ramp-up is complete, VTT is limited to a maximum of 0.95 V.
 - Vref is $VDDQ/2$.

Or

- Apply VDD before or simultaneously with VDDQ, without any slope reversal.
 - Apply VDDQ before or simultaneously with VTT and Vref, without any slope reversal.
 - Voltage levels on all pins except VDD, VDDQ, VSS, and VSSQ must be less than or equal to VDD and VDDQ, and must be greater than or equal to VSS and VSSQ.
2. After RESET# is de-asserted, wait at least 500 μ s before driving CKE HIGH. During this time, the DRAM will begin internal state initialization; this process is independent of the external clock.
 3. Before CKE is activated (HIGH), the clocks (CK, CK#) must be started and stable for at least 10 ns or 5 tCK (whichever is larger). Since CKE is a synchronous signal, the corresponding setup time tIS must be satisfied. Additionally, before CKE activation, a NOP or deselect command must be issued in accordance with the clock (meeting tIS setup time). Once CKE is driven HIGH after reset completion, it must remain HIGH until the initialization sequence is complete, including the end of tDLLK and tZQint.
 4. While RESET# is asserted, the DDR3 DRAM will maintain its pin terminations in a high-impedance state. Additionally, after RESET# is de-asserted, the DRAM still maintains its pin terminations in a high-impedance state until CKE is registered HIGH. ODT input signals are in a don't-care state during tIS cycles until CKE is registered HIGH. When CKE is registered HIGH, ODT input signals can be statically held HIGH or LOW. If RTT_NOM is enabled in register MR1, ODT input signals must be statically held LOW. In all cases, ODT input signals remain static until the power-up initialization sequence is complete, including the end of tDLLK and tZQint.
 5. After CKE is registered HIGH, a minimum of the reset CKE exit time tXPR must be waited before issuing the first MRS command to load the mode registers. [tXPR = max(tXS, 5 tCK)].
 6. Issue an MRS command to load all application configurations into register MR2. (Ensure that when issuing the MRS command to configure register MR2, BA0 and BA2 are set LOW, and BA1 is set HIGH.)
 7. Issue an MRS command to load all application configurations into register MR3. (Ensure that when issuing the MRS command to configure register MR3, BA2 is set LOW, and BA0 and BA1 are set HIGH.)

BA2 is set to LOW, BA0 and BA1 are set to HIGH).

8. Issue MRS command to load all application configurations into register MR1 and configure the DLL. (Ensure DLL enable: A0 set to LOW, BA0 set to HIGH, BA1 and BA2 set to LOW).
9. Issue MRS command to load all application configurations into register MR0 and configure DLL reset. (Ensure DLL reset: A8 set to HIGH, BA0, BA1, BA2 set to LOW).

A8 set to HIGH, BA0, BA1, BA2 set to LOW.

10. Issue ZQCL command to start ZQ calibration.
11. Wait for tDLLK and tZQinit to complete.
12. DDR3 SDRAM initialization is complete and ready for normal operation. Power-up initialization, reset sequence:

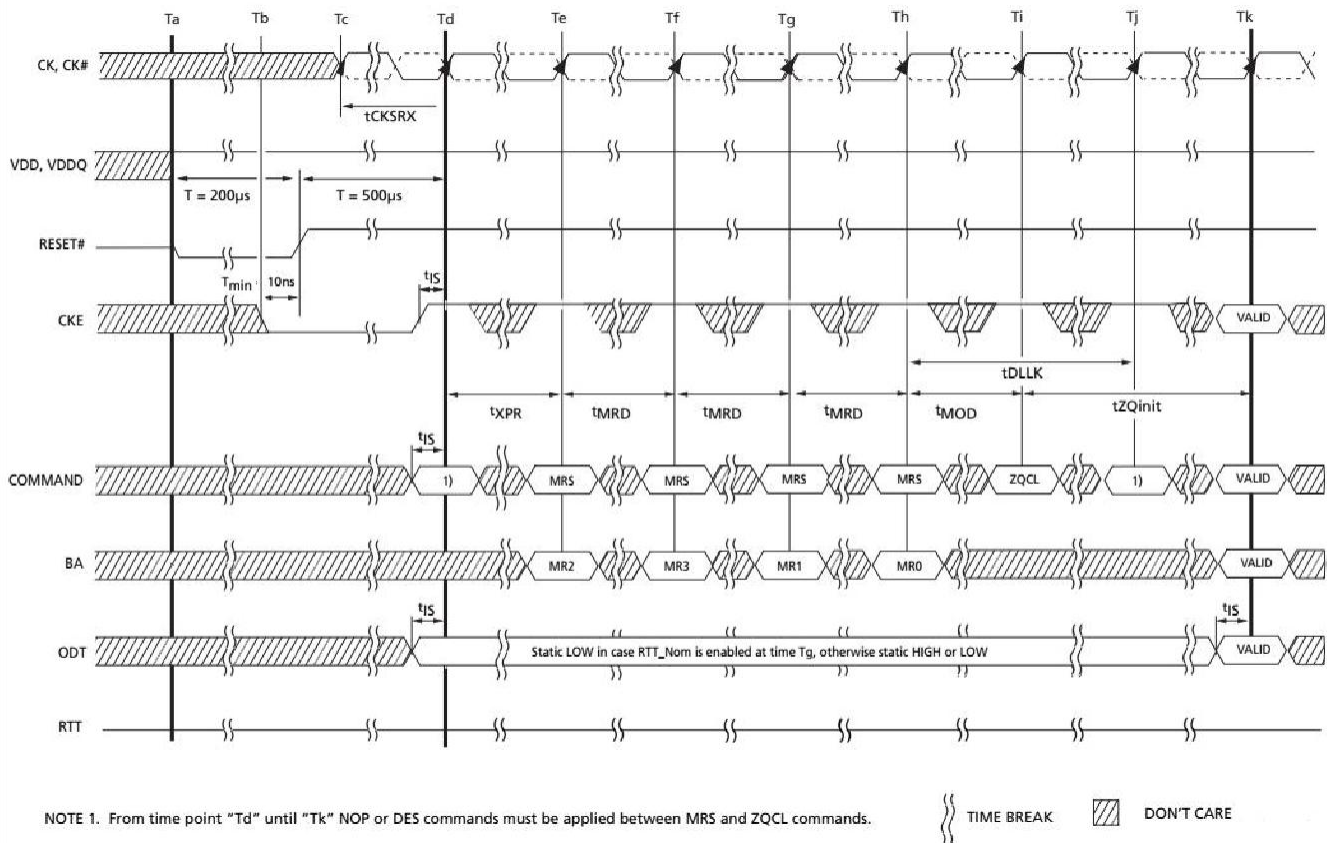
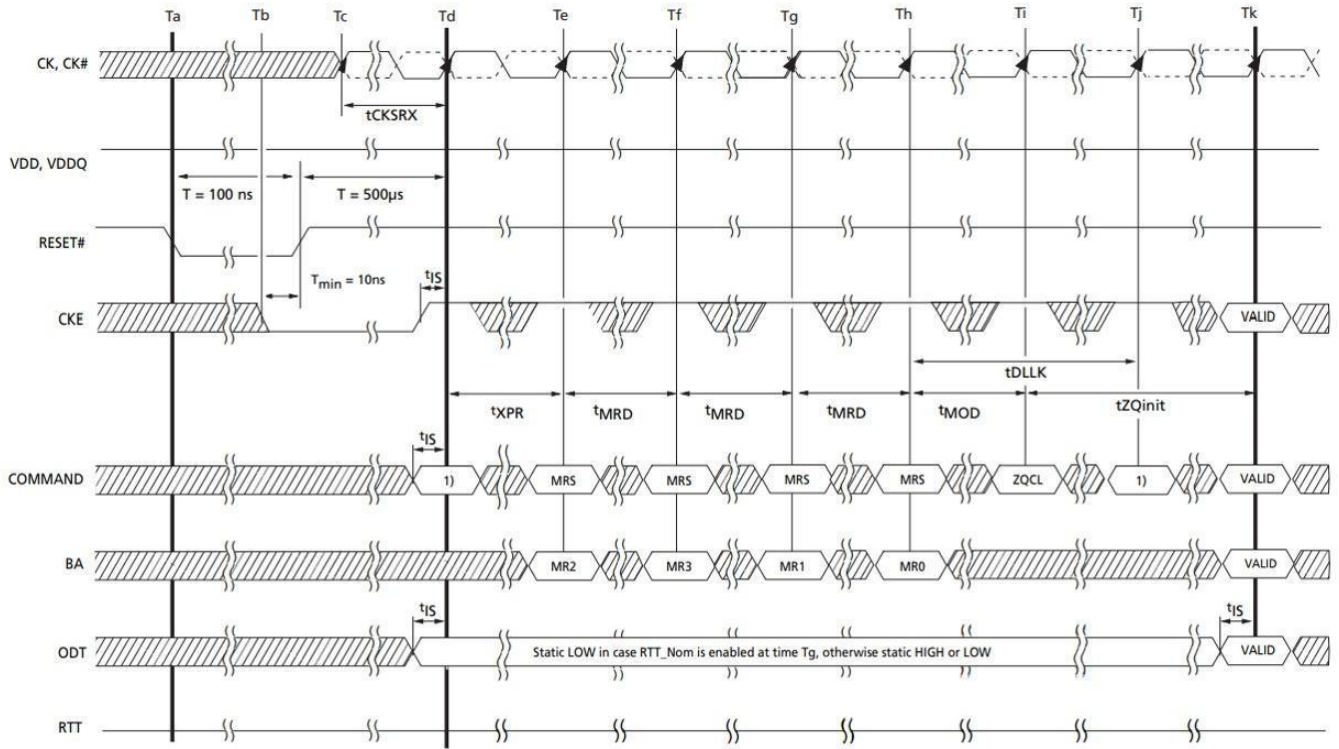


Figure 4 Initialization Reset Sequence Diagram

Reset Procedure with Power Stable

During initialization without power interruption, the reset operation sequence is as follows.

1. When reset is required, ensure RESET# is below $0.2 \times VDD$ (all other inputs may be at any level). RESET# must be held for at least 100 ns. Before RESET# is released (minimum 10 ns), CKE should be driven LOW.
2. Follow steps 2 through 11 of the power-up initialization sequence.
3. Reset procedure completed. DDR3 SDRAM is ready for normal operation. Normal power-up reset sequence:

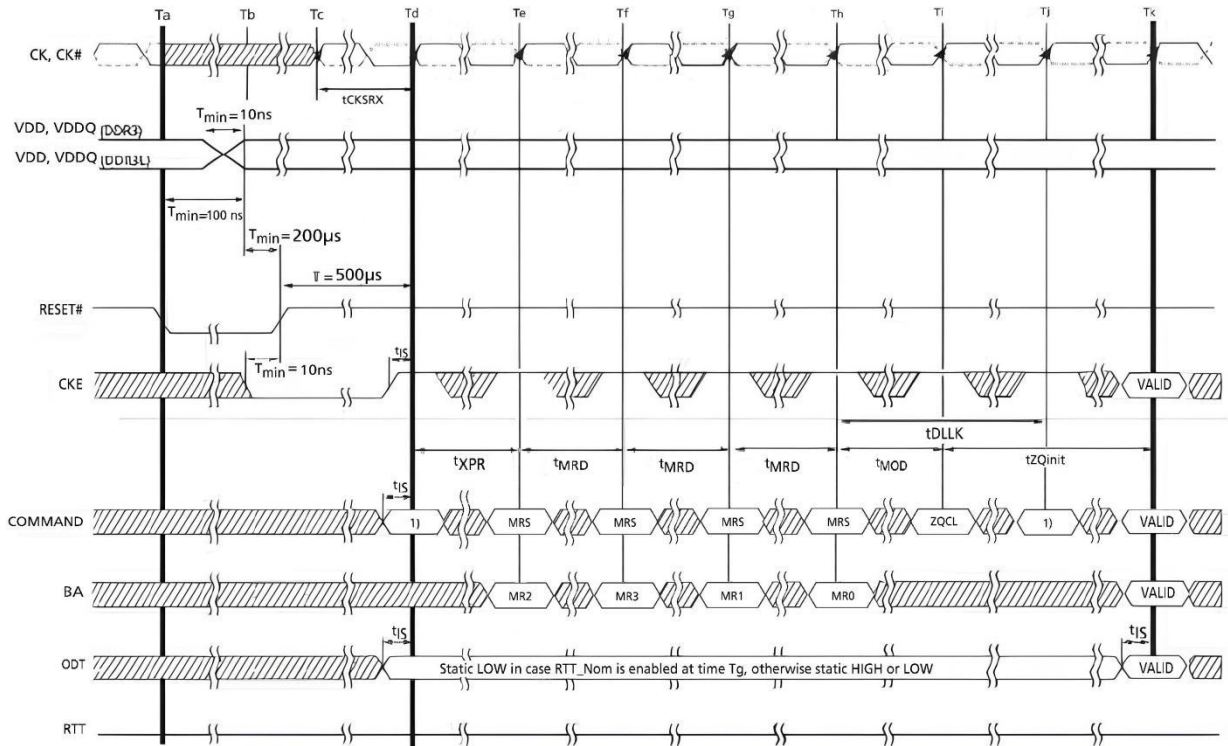


NOTE 1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK DON'T CARE

Figure 5 Power-Up Reset Timing Diagram

VDD/VDDQ Voltage Ramp Timing:



NOTE 1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK DON'T CARE

Figure 6 VDD/VDDQ Voltage Ramp Timing Diagram

Register Definition

Mode Register Configuration

For application flexibility, the DDR3 SDRAM provides four programmable mode registers, which the user can program via the Mode Register Set (MRS) command. Since the default values of the Mode Registers (MR#) are not defined, the contents of the mode registers must be fully initialized and/or re-initialized, e.g., after power-up or reset, for proper operation. In addition, the mode register contents can be changed by re-executing the MRS command during normal operation. When programming the mode registers, all address fields within the accessed mode register must be redefined when the MRS command is issued, even if the user chooses to modify only a subset of the MRS fields. The MRS command and DLL reset do not affect the array contents, meaning that these commands can be executed at any time after power-up without affecting the array contents.

The mode register set command cycle time, t_{MRD} , is the time required to complete a write operation to the mode register. It is the minimum time required between two MRS commands, as shown below.

t_{MRD} Timing:

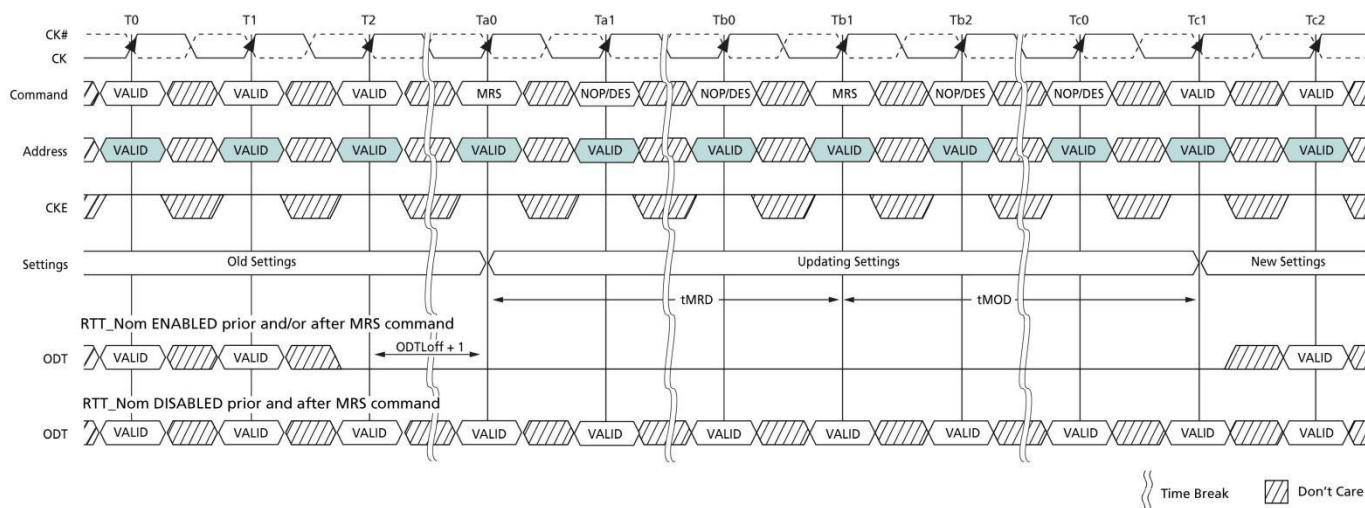


Figure 7 t_{MRD} Timing Diagram

The delay time from an MRS command to a non-MRS command, t_{MOD} , is the minimum time required from an MRS command to a non-MRS command other than NOP and DES, from

the MRS command to a non-MRS command other than NOP and DES, as shown in the figure below.

t_{MOD} Timing:

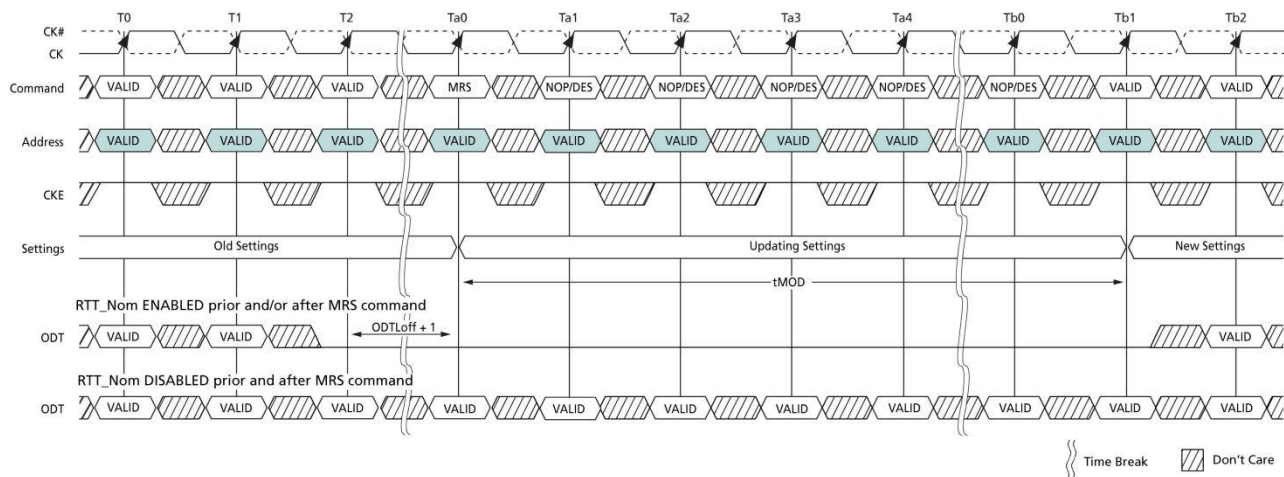


Figure 8 tMOD Timing Diagram

During normal operation, as long as the DRAM is in the idle state, the same command and timing requirements can be used to change the mode register contents. That is, all banks are in the precharge state, t_{RP} is satisfied, all burst transfers have completed, and CKE remains high before writing to the mode register. The mode register is divided into different fields by function.

5.1.1 Mode Register MR0

Mode Register MR0 is used to configure various operating modes of the DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, write recovery time (WR), and precharge power-down DLL control, including vendor-specific options to make the DDR3 SDRAM suitable for various applications. Writing to the mode register is determined by setting CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2 low while controlling the address pin states according to the figure below.

MR0 Definition

Table 6 MR0 Definition

BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	MRS	0	0	0	PD	WR				DLL	TM	CL			BT	CL	BL	

MRS Mode: MRS

Table 7 MRS Mode Information

BA1	BA0	MRS Command
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Precharge Power-Down:
PD

Table 8 DLL Control in Precharge Power-Down

A12	DLL Control in Precharge Power-Down
0	Slow Exit (Low Power)
1	Fast Exit (Normal Operation)

Read Burst Type: BT

Table 9 Read Burst Type

A3	Read Burst Type
0	Sequential
1	Interleaved

Burst Length: BL

Table 10 Burst Length

A1	A0	BL
0	0	8 (Fixed)
0	1	BC4 or 8 (OTF)
1	0	BC4 (Fixed)
1	1	Reserved

Write Recovery for Auto
Precharge: WR

Table 11 Auto Precharge Write Recovery (WR) Information

A11	A10	A9	WR (Cycles)
0	0	0	16
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

CAS Latency: CL

Table 12 CAS Latency Information

A6	A5	A4	A2	CAS Latency Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	14
0	1	1	1	15
1	0	0	1	16

DLL Reset: DLL

Table 13 DLL Reset

A8	DLL Reset
0	No
1	Yes

Test Mode: TM

Table 14 Test Mode (TM)

A7	Mode
0	Normal
1	Test

1. BA2, A13, A14, and A15 are RFU and must be programmed to 0 during MRS.
2. The minimum clock cycles for WR (write recovery for auto precharge) is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up: $WR_{min}[cycles] = \text{round}(tWR/tCK)$. The WR value in the mode register must be programmed to be equal to or greater than WRmin. The programmed WR value is used together with tRP to determine tDAL.
3. This table only provides the CAS latency coding. For actual supported CAS latencies, refer to the speed bin table for each frequency.
4. This table only provides the write recovery coding. For actual write recovery time, refer to the AC timing table.

Burst Length, Type, and Command

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected by bit A3 as shown in the MR0 definition above. The order of accesses within the burst is determined by the burst length, burst type, and starting column address. The burst length is defined by bits A0, A1. Burst length options (including fixed BC4, fixed BL8, and BC4 or BL8 allowed in on-the-fly mode) are selected via A12/BC, synchronized with registration of the read or write command.

Table 15 Burst Sequencing Generation Rules

Burst Length	Read/Write Command	Starting Column Address (A2,A1,A0)	Burst Type: Sequential (Decimal) A3 = 0	Burst Type: Interleaved (Decimal) A3 = 1	Notes
4 Truncated	Read	0,0,0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1,2,3
		0,0,1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	
		0,1,0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	
		0,1,1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	
		1,0,0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	
		1,0,1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	
		1,1,0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	
		1,1,1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	
	Write	0,V,V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1,2,4,5
		1,V,V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	

BL8	Read	0,0,0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0,0,1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	
		0,1,0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	
		0,1,1	3,0,1,2,7,3,5,6	3,2,1,0,7,6,5,4	
		1,0,0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	
		1,0,1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	
		1,1,0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	
		1,1,1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	
	Write	V,V,V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2,4

Note:

1. When the burst length is fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than in BL8 mode. This means that two clock cycles are required to achieve the tWR and tWTR starting points. In on-the-fly mode, when the burst length is selected via A12/BC, the start time of the internal write operation is the same as that of a burst-8 write operation. This means that during on-the-fly control, two clock cycles are no longer required to achieve the tWR and tWTR starting points.
2. Bits 0–7 are determined by the value of CA[2:0]; the first data read within the burst cycle corresponds to these bits.
3. T: Data and strobe output drivers are in high-impedance state.
4. V: Logic valid level (0 or 1), but the corresponding buffer input ignores the actual signal level on the pin.
5. X: Don't care.

5.1.1.1 CAS Latency

As shown in the MR0 definition, CAS latency is defined by MR0(A9–A11). CAS latency is the delay, in clock cycles, between the internal read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half-clock latency. The global read latency (RL) is defined as additive latency (AL) plus CAS latency (CL): $RL = AL + CL$.

Test Mode

For normal operation mode selection, MR0(A7 = 0) is required and all other bits of the register must be set to the values shown in the MR0 definition. Programming A7 to 1 places the DDR3 SDRAM into test mode, which is for DRAM manufacturer use only. If A7=1, no operation or functionality is guaranteed.

5.1.1.2 DLL Reset

The DLL reset bit is self-clearing, meaning it returns to a value of "0" after the DLL reset function is issued. Once the DLL is enabled, the DLL reset becomes

used. Whenever the DLL reset function is used, other DLL functions (e.g., read command or ODT) must not be used until after tDLL clock cycles.

synchronous operation)

5.2.2.4 DLL Write Recovery

The tWR programming value is determined by the MR0 register (A9, A10, A11), used for the auto precharge function, and together with tRP determines the minimum clock cycle of tDAL (write recovery delay for auto precharge). The programmed tWR value (in clock cycles) must be greater than or equal to the result of the minimum tWR (in ns) divided by tCK, rounded up: $tWR\_min[cycles] = \text{Roundup}(tWR\_min\_ns / tCK)$.

= $\text{Roundup}(tWR\_min\_ns / tCK)$. The programmed tWR value must be greater than or equal to the number of clock cycles corresponding to the minimum tWR.

5.2.2.5 DLL Precharge Power-Down

The MR0 register (A12) is used for DLL precharge power-down mode selection. When MR0(A12 = 0) or "slow exit", the DLL is frozen after entering precharge power-down (to save power), and upon exit, a wait of tXPDLL clock cycles is required before the next valid command. When MR0(A12 = 1) or "fast exit", the DLL remains active after entering precharge power-down, and upon exit, a wait of tXP clock cycles is required before the next valid command.

5.1.2 Mode Register MR1

Mode Register MR1 stores data for enabling or disabling the DLL, output drive strength, Rtt_Nom impedance, additive latency, write leveling enable, and Qoff. The Mode Register MR1 is written by setting CS#, RAS#, CAS#, and WE# low, BA0 high, BA1 and BA2 low, while controlling the address pin states according to the figure below.

MR1 Definition

Table 16 MR1 Definition

BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	0	Qoff	TDQS	0	Rtt	0	WL	Rtt	ODS	AL		Rtt	ODS	DLL

DLL Selection: DLL

Table 17 DLL Selection

A0	DLL
0	Enable
1	Disable

Qoff Selection: Qoff

Table 18 Qoff Selection

A12	Qoff
0	Output Buffer Enabled
1	Output Buffer Disable

TDQS Mode: TDQS

Table 19 TDQS Mode

A11	TDQS
0	Disable
1	Enable

Write Leveling Mode: WL

Table 20 Write Leveling Mode (WL)

A7	Write leveling
0	Disable
1	Enable

Additive Latency: AL

Table 21 Additive Latency (AL)

A4	A3	AL
0	0	0: Disabled
0	1	CL-1
1	0	CL-2
1	1	Reserved

Output Driver Strength:
ODS

Table 22 Output Driver Strength (ODS)

A5	A1	Write leveling
0	0	RZQ/6
0	1	RZQ/7
1	0	Reserved
1	1	Reserved

Nominal Termination
Value: Rtt_Nom

Table 23 Nominal Termination Value (Rtt_Nom)

	A6	A2	Rtt_Nom
0	0	0	ODT Disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12
1	0	1	RZQ/8
1	1	0	Reserved
1	1	1	Reserved

1. BA2 and A8, A10, A13, A14, A15 are RFU and must be programmed to 0 during MRS.
2. Outputs Disabled – DQ, DQS, DQS#.
3. RZQ = 240.
4. In write leveling mode, when MR1 bit 12 = 1 and bit 7 = 1, all RTT_Nom settings are allowed; in write leveling mode, when MR1 bit 12 = 0 and bit 7 = 1, only RTT_Nom settings of RZQ/2, RZQ/4, and RZQ/6 are allowed.
5. If RTT_Nom is used during write operations, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

5.1.2.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and when returning to normal operation after DLL disable. Mode

Register MR1(A0=0) for normal operation (DLL on). The DLL is automatically disabled when entering self-refresh operation and automatically re-enabled upon exit from self-refresh. When the DLL is enabled and subsequently reset, it is necessary to wait tDLLK clock cycles before issuing a read or synchronous ODT command to allow the internal clock to synchronize with the external clock. Failure to wait for synchronization to occur may result in tDQSK, tAON, or tAOF parameters not being met. During tDLLK, CKE must be continuously held HIGH. DDR3 SDRAM does not require the DLL for any write operation, except when RTT_WR is enabled and ODT operation requires the DLL. For details on DLL disable operation, see the DLL Off Mode table. Direct ODT function is not supported during DLL Off mode. The on-die termination function is disabled; in DLL Off mode, the ODT pin must be held LOW continuously and/or the Rtt_Nom control bits {A9, A6, A2} must be programmed to (0,0,0) via MRS commands.

Dynamic ODT function is not supported in DLL Off mode. The user must set Rtt_WR using the MRS command by programming register MR2(A10, A9) to (0,0) to disable dynamic ODT.

Output Driver Impedance Control

The output driver impedance of DDR3 SDRAM devices is selected by mode register MR1 (A1 and A5) as shown in the MR1 Definition figure.

ODT Rtt Values

DDR3 SDRAM provides two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom can be programmed in mode register MR1. A separate value (Rtt_WR) can be programmed in register MR2 to enable a unique Rtt value when ODT is enabled during write operations. Rtt_WR can be used during write operations even when Rtt_Nom is disabled.

5.1.2.2 Additive Latency (AL)

Additive latency (AL) operation is supported to make the command and data bus efficient for sustainable bandwidth in DDR3 SDRAM. In this operation, DDR3 SDRAM allows a read or write command (with or without auto-precharge) to be issued immediately after the activate command. The command is held for a time equal to the additive latency (AL) before being issued internally to the device. Read latency (RL) is controlled by the sum of AL and the register-set CAS latency (CL). Write latency (WL) is controlled by the sum of AL and the register-set CAS write latency (CWL). The AL register options are shown in the table above.

Write Leveling

For better signal integrity, DDR3 memory modules use a fly-by topology for command, address, control signals, and clocks. The fly-by topology helps reduce the number and length of stubs, but otherwise causes a propagation time skew between the clock and strobe for each DRAM in the memory. This makes it difficult for the controller to meet the tDQSS, tDSS, and tDSH specifications. Therefore, the controller should support "write leveling" in DDR3 SDRAM to compensate for the skew.

Output Disable

DDR3 SDRAM output enable/disable can be controlled by mode register MR1 bit 12. As shown in the mode register MR1 definition, when this feature is enabled (A12 = 1), all output pins (DQ, DQS, DQS#, etc.) are disconnected from the output drivers, thereby removing any load from the output drivers. This feature may be useful, for example, when measuring module

power. For normal operation, A12 should be set to "0".

ODT Enable

TDQS (Termination Data Strobe) is a feature of ×8 DDR3 SDRAM that provides additional termination resistor outputs that may be useful in certain system configurations.

When enabled via Mode Register MR1, the TDQS and TDQS# pins have the same termination resistor function as the DQS and DQS# pins.

Unlike the RDQS function of DDR2 SDRAM, TDQS only provides a termination resistor function. TDQS does not provide the data strobe function of RDQS.

The TDQS and DM functions share the same pin. When the TDQS function is enabled via the Mode Register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided.

The TDQS function is only available in ×8 DDR3 SDRAM. For ×16 configurations, it must be disabled via Mode Register MR1 with A11=0. ~~XX~~

Table 24 TDQS, TDQS# Function Table

MR1(A11)	DM/TDQS	NU/TDQS#
0 (TDQS Disabled)	DM	Hi-Z
1 (TDQS Enable)	TDQS	TDQS#

5.1.3 Mode Register MR2

Mode Register MR2 stores data for controlling refresh-related features, RTT_WR impedance, and CAS write latency. MR2 is written by setting CS#, RAS#, CAS#, WE# low, BA1 high, BA0 and BA2 low, while according to the following figure

Control the state of address pins.

MR2 Definition

Table 25: MR2 Definition

BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	0	0	Rtt_WR	0	SRT	ASR		CWL			0	0	0

Dynamic ODT:

RTT_WR

Dynamic ODT (Rtt_WR) Information

A10	A9	Rtt_WR
0	0	Dynamic ODT Off
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

Temperature-Controlled
Self-Refresh: SRT

Temperature Compensated Self-Refresh (SRT)

A7	SRT
0	Normal
1	Extended

Auto Self-Refresh (ASR)

Self-Refresh: ASR

A6	ASR
0	Manual Self-Refresh
1	ASR Enable

CAS Write Latency: CWL

Table 29 CAS Write Latency (CWL) Information Table

A5	A4	A3	CWL
0	0	0	5($t_{CK} \geq 2.5ns$)
0	0	1	6($2.5ns > t_{CK} \geq 1.875ns$)
0	1	0	7($1.875ns > t_{CK} \geq 1.5ns$)
0	1	1	8($1.5ns > t_{CK} \geq 1.25ns$)
1	0	0	9($1.25ns > t_{CK} \geq 1.07ns$)
1	0	1	10($1.07ns > t_{CK} \geq 0.935ns$)
1	1	0	11($0.935ns > t_{CK} \geq 0.833ns$)
1	1	1	12($0.833ns > t_{CK} \geq 0.75ns$)

1. BA2, A5, A8, A11, A12, A13 are RFU and must be programmed to 0 during MRS.
2. Even if Rtt_Nom is disabled, the Rtt-WR value can be used during write operations. Dynamic ODT is not available during write leveling.

5.1.3.1 CAS Write Latency

CAS write latency is defined by MR2(A3, A4, A5). CAS write latency is the delay, in clock cycles, between the internal write command and the first bit of valid input data. DDR3 DRAM does not support any half-clock latency. The total write latency (WL) is defined as additive latency (AL) plus CAS write latency (CWL); $WL = AL + CWL$.

For more information on supported CWL and AL settings based on operating clock frequency, refer to the Speed Bin. For detailed write operation, refer to the WRITE operation.

5.1.3.2 Auto Self-Refresh (ASR) and Temperature-Controlled Self-Refresh (SRT)

The DDR3 SDRAM must support self-refresh operation across all supported temperatures. Applications that require self-refresh operation over the extended temperature range must use the ASR feature or program the SRT feature bits appropriately.

DDR3 SDRAM Optional Features: Users should refer to the DRAM supplier datasheet and/or memory SPD to determine whether the DDR3 SDRAM supports the following options or requirements mentioned in this material. For more details, refer to the "Extended Temperature Usage Manual." The DDR3 SDRAM must support self-refresh operation across all supported temperatures. Applications that require self-refresh operation over the extended temperature range must use the optional ASR feature or program the SRT feature bits appropriately.

5.1.3.3 Dynamic ODT (Rtt_WR)

The DDR3 SDRAM introduces a new feature called "Dynamic ODT." In certain applications, to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the DDR3 SDRAM without issuing an MRS command. Dynamic ODT settings are configured via bits A9 and A10 of Mode Register MR2. In write leveling mode, only Rtt_Nom is available. For details on dynamic ODT operation, refer to "Dynamic ODT."

5.1.4 Mode Register MR3

Mode Register MR3 controls the multipurpose register. The mode register MR3 is written by setting CS#, RAS#, CAS#, and WE# LOW, setting BA1 and BA0 HIGH, and BA2 LOW, while controlling the address pin states according to the following figure.

MR3 Definition

Table 30 MR3 Definition

BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	0	0	0	0	0	10	0	0	0	0	0	108	MPR	MPR Location	

Multi-Purpose Register (MPR)

Table 31 Multi-Purpose Register (MPR)

A2	MPR
0	Normal Operation
1	MPR Data Stream

Multi-Purpose Register Data Order: MPR Location

Table 32 Multi-Purpose Register Data Order (MPR Location) Information

A1	A0	MPR Read Mode
0	0	Predefined Pattern
0	1	RFU
1	0	RFU
1	1	RFU

1. BA2, A3–A15 are RFU and must be programmed to 0 during MRS.
2. The predefined pattern will be used for read operations.
3. When MPR control is set to normal operation (Mode Register MR3 A2 = 0), Mode Register MR3 A1, A0 are ignored.

Multi-Purpose Register

The Multi-Purpose Register (MPR) function is used to read a predefined system timing calibration bit sequence. To enable the MPR, a Mode Register Set (MRS) command must be issued to Mode Register MR3 with A2=1. Before issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP satisfied). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi-Purpose Register (MPR). When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 A2 =0). During MPR enable mode, power-down mode, self-refresh, and any other non-RD/RDA commands are not allowed. Reset function is not supported.

Used in enable mode.

The Multi-Purpose Register (MPR) function is used to read a predefined system timing calibration bit sequence.

MPR Block Diagram

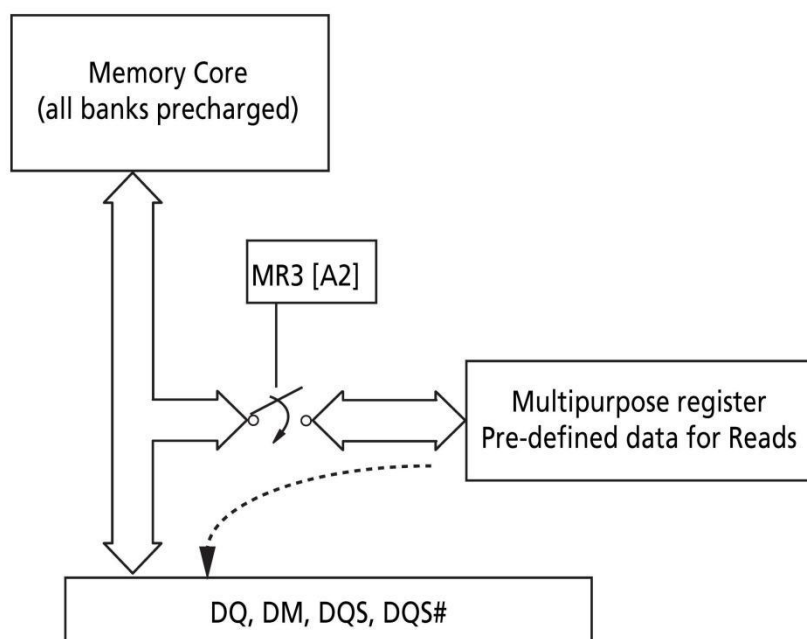


Figure 9 MPR Block Diagram

MPR Function
Definition:

Table 23 MPR Function Definition

MR3 A2	MR3 A[1:0]	Function
MPR	MPR_Loc	
0b	Don't Care (0 or 1)	Normal operation, no MPR transaction All subsequent reads will come from the DRAM array All subsequent writes will go to the DRAM array
1b	MPR mode enable, MPR page defined by MR3 A[1:0] Command	MPR mode enable, MPR page defined by MR3 A[1:0] (Merged into previous entry)

MPR Functional Description

- During MPR read operation, all DQ pins output the same single-bit data.
- Registered read is BL8 mode:✕

DQ[0] drives data from the MPR register.

DQ[7:1] drive the same data as DQ[0], or all are set to 0.

- Registered Read for 16 mode:✕

DQL[0] and DQU[0] drive data from the MPR register.

DQL[7:1] and DQU[7:1] drive the same information as DQL[0], or are set to 0b.

- All MPR registers, when addressed during a Multi-Purpose Register read:

BA[2:0]: Don't care

A[1:0]: A[1:0] must equal '00'. The read burst order within a nibble is fixed. A[2]:

For BL = 8, A[2] must equal 0b, and the burst order is fixed to [0,1,2,3,4,5,6,7].

For burst chop 4, the burst order is switched on a nibble basis: A[2] = 0b, burst order: 0,1,2,3. A[2] = 1b, burst order: 4,5,6,7.

A[9:3]: Don't Care

A10/AP: Don't

Care

A12/BC: If enabled in MR0, selects burst chop mode in on-the-fly mode.

A11, A13, A14... (if available): Don't Care

- Normal interface functions during register read:

Supports two burst orders, selected by setting A2 and A[1:0]=00b.

Supports read burst chop (by MRS setting or dynamic selection via A12/BC pin)

All other address bits (including all column address bits including A10, all bank address bits) are ignored by the DDR3 SDRAM. Normal read latency and AC timing apply.

- DLL must be locked before MPR read.

Note: Burst order bit 0 is assigned to the LSB (Least Significant Bit) of the MPR, and burst order bit 7 is assigned to the MSB (Most Significant Bit) of the selected MPR.

valid bit).

5.2 DDR3 SDRAM Command Definitions and Operations

Command Truth Table

Table 34 Command Truth Table

Function	Abbreviation	CKE		CS #	RA S#	CA S#	WE #	BA[2 : 0]	A15-A 13	A1 2	A10/AP	A[11,9: 0] 1, 9:0]	Notes
		Pre v cyc le	Next Cycl e										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP-Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9, 12
		L	H	L	H	H	H	V	V	V	V	V	7,8,9, 12
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge All Banks Banks	PREA	H	H	L	L	H	L	V	V	V	V	V	
Bank Active	ACT	H	H	L	L	H	H	BA	Row Address(RA)				
Write (Fixed BL8 or BC4) or BC4)	WR	H	H	L	H	L	L	BA	BFU	V	L	CA	
Write(BC4 on the fly)	WRS4	H	H	L	H	L	L	BA	BFU	L	L	CA	

Write(BL8 on the fly)	WRS8	H	H	L	H	L	L	BA	BFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	BFU	V	H	CA	
Write with Auto Precharge (BC4 on the fly)	WRA S4	H	H	L	H	L	L	BA	BFU	L	H	CA	
Write with Auto Precharge (BL8 on the fly)	WRA S8	H	H	L	H	L	L	BA	BFU	H	H	CA	
Read(Fixed BL8 or BC4)	RD	H	H	L	H	L	L	BA	BFU	V	L	CA	
Read(BC4 on the fly)	RDS4	H	H	L	H	L	L	BA	BFU	L	L	CA	
Read(BL8 on the fly)	RDS8	H	H	L	H	L	L	BA	BFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	L	BA	BFU	V	L	CA	
Read with Auto Precharge(BC4 on the fly)	RDA S4	H	H	L	H	L	L	BA	BFU	L	H	CA	
Read with Auto Precharge (BL8 on the fly)	RDA S8	H	H	L	H	L	L	BA	BFU	H	H	CA	
No operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselect	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
		H	L	H	X	X	X	X	X	X	X	X	6,12
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
		L	H	H	X	X	X	X	X	X	X	X	6,12
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Note:

- On the rising edge of the clock, all DDR3 SDRAM commands are determined by the state of CS#, RAS#, CAS#, WE#, and CKE signals. The high-order BA bits, RA, and CA depend on the chip density and configuration.

2. RESET# is an active-low asynchronous reset command and must be held HIGH during normal operation.
3. Bank Address (BA) selects the specified bank. For (E)MRS, BA selects an (extended) mode register.
4. "V" indicates "H or L (valid logic level)", "X" indicates "Don't Care (any logic level)".
5. Burst read and write operations cannot be terminated or interrupted. The burst length (BL) in fixed or on-the-fly mode is defined by MRS.
6. Power-down mode does not perform any refresh operations.
7. The ODT state does not affect the states described in this table. ODT functionality is not available during self-refresh.
8. Self-refresh exit is asynchronous.
9. VREF (VrefDQ and VrefCA) must be maintained during self-refresh operation.
10. The 'No Operation' command should be used when the DDR3 SDRAM is in an idle or waiting state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. The 'No Operation' command does not terminate a previously executed operation, such as a burst read or write cycle.
11. The deselect command performs the same function as the no operation command.
12. For more details on CKE transitions, refer to the CKE truth table.

5.2.1 CKE Truth Table

Table 35 CKE Truth Table

Current State	CKE		Command (N)RAS#,CAS#,WE#,CS#	Operation (N)	Notes
	Prev Cycle (N-1)	Next Cycle (N)			
Power Down	L	L	X	Maintain Power Down	14,15
	L	H	DESELECT or NOP	Power Down Exit	11,14
Self Refresh	L	L	X	Maintain Self Refresh	15,16
	L	H	DESELECT or NOP	Self Refresh Exit	8,12,16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	11,13,14
Reading	H	L	DESELECT or NOP	Power Down Entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power Down Entry	11,13,14,17
Precharge	H	L	DESELECT or NOP	Power Down Entry	11,13,14,17
Refresh	H	L	DESELECT or NOP	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	11,13,14,18
	H	L	REFRESH	Self Refresh	9,13,18

Note:

1. CKE(N) is the logic state of CKE at clock edge N; CKE(N-1) is the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM prior to clock edge N.

3. COMMAND(N) is the command registered at clock edge N, and ACTION(N) is the result of COMMAND(N); ODT is not included here.
4. Unless otherwise explicitly stated elsewhere in this document, all states and sequences not shown are illegal or reserved.
5. The state of ODT does not affect the states described in this table. ODT functionality is not available during self-refresh.
6. CKE must be registered with the same value on consecutive positive clock edges for tCKEmin. CKE must remain valid for the entire duration required to achieve the tCKEmin clocks for registration. Therefore, after any CKE transition, CKE may not transition to its valid level for a period of tIS + tCKEmin + tIH.
7. DESELECT and NOP are defined in the command truth table.
8. When exiting self-refresh, the DESELECT or NOP command must be issued on every clock edge for tXS clock cycles. Only when tXSDLL

After the clock cycle, a read or ODT command may be issued.

9. Self-refresh mode can only be entered from the all-banks-idle state.
10. Must be a valid command as defined in the command truth table.
11. The only valid commands for power-down entry and exit are NOP and DESELECT.
12. The only valid commands for self-refresh exit are NOP and DESELECT.
13. Self-refresh cannot be entered during a read or write operation.
14. Precharge power-down does not perform any refresh operations.
15. 'X' indicates a 'don't care' in self-refresh and power-down (including VREF floating). It also applies to address pins.
16. VREF (VREF_DQ and VREF_CA) must be maintained during self-refresh operation.
17. If all banks are closed at the end of a read, write, or precharge command, the device enters precharge power-down; otherwise, it enters active power-down.
18. The idle state is defined as all banks closed (tRP, tDAL, etc. clock cycles satisfied), no data burst in progress, CKE HIGH, all timing for previous operations satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc. clock cycles), and all self-refresh exit and power-down exit parameters satisfied (tXS, tXP, tXPDLL, etc. clock cycles).

5.2.2 No Operation (NOP) Command

The No Operation (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP (CS# is LOW; RAS#, CAS#, and WE# are HIGH).

Driven HIGH to prevent registration of unwanted commands during idle or wait states; operations already in progress are not affected.

5.2.3 Deselect Command

The Deselect function (Deselect, CS# is HIGH) prevents the DDR3 SDRAM from executing new commands. When the DDR3 SDRAM is deselected, operations already in progress are not affected.

5.2.4 DLL-off Mode

Entering DDR3 DLL-off mode by setting bit A0 of Mode Register MR1 to '1'; this disables the DLL until

bit A0 is set back to '0'. Bit A0 of Mode Register MR1, which controls the DLL, can be toggled during initialization or later.

The DLL-off mode operations listed below are an optional feature of DDR3. The maximum clock frequency in DLL-off mode is specified by the parameter t_{CKDLL_off}

There is no minimum frequency requirement other than meeting the refresh interval t_{REFI} .

Due to latency counters and timing restrictions, only one CAS latency (CL) value is supported in MR0, and only one CAS write latency (CWL) value is supported in Mode Register MR2. DLL-off mode is only intended to support settings with CL = 6 and CWL = 6.

DLL-off mode affects the read data clock-to-data strobe relationship (t_{DQSQ}), but does not affect the data strobe-to-data relationship (t_{DQSQ} ,

t_{QH}). Special care is required to align the read data to the controller's time domain.

Compared to DLL-on mode, where t_{DQSQ} starts from the rising clock edge after the read command (AL+CL) cycles, in DLL-off mode t_{DQSQ} starts (AL+CL-1) cycles after the read command. Another difference is that t_{DQSQ} may not be less than t_{CK} (it may even be greater than t_{CK}), and the difference between $t_{DQSQmin}$ and $t_{DQSQmax}$ is significantly larger than in DLL-on mode.

The timing relationship for a READ operation in DLL-off mode is shown in the following timing diagram (CL=6, BL=8).

READ Operation Timing in DLL-off Mode

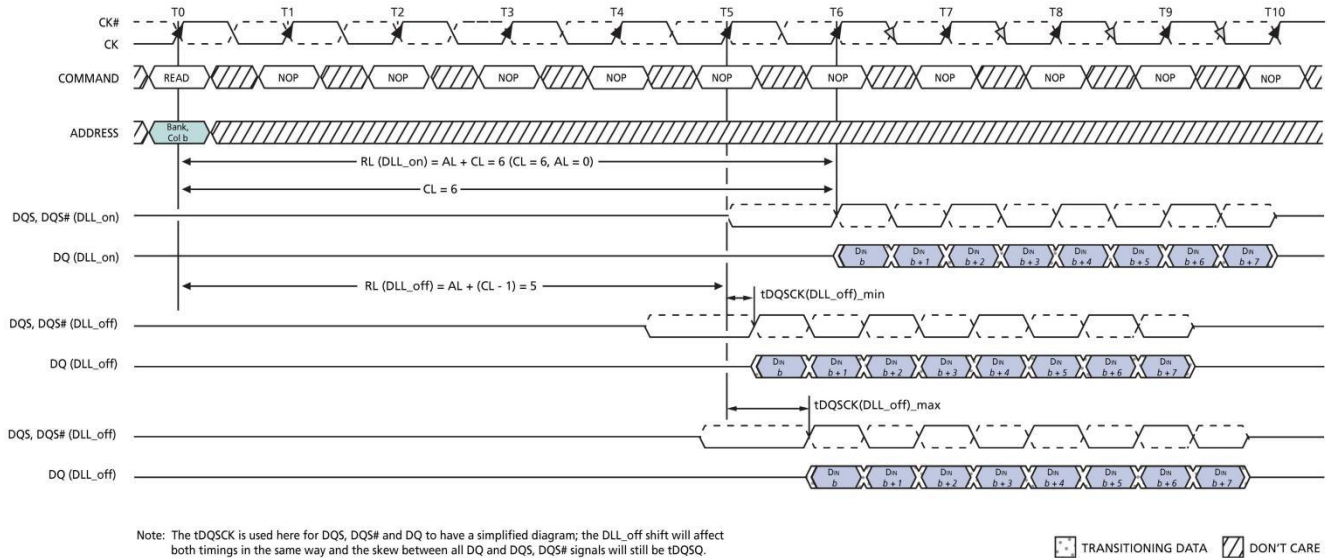


Figure 10 - READ Operation Timing Relationship

5.2.4.1 DLL On/Off Switching Procedure

By setting mode register MR1 A0 to '1', the DDR3 DLL disable mode is entered; this disables the DLL for subsequent operations until

A0 is set back to '0'.

DLL Enable to DLL Disable Procedure:

To switch from DLL enable to DLL disable, the frequency must be changed during self-refresh according to the following procedure:

1. Starting from the idle state (all banks are precharged, all timing is complete, and

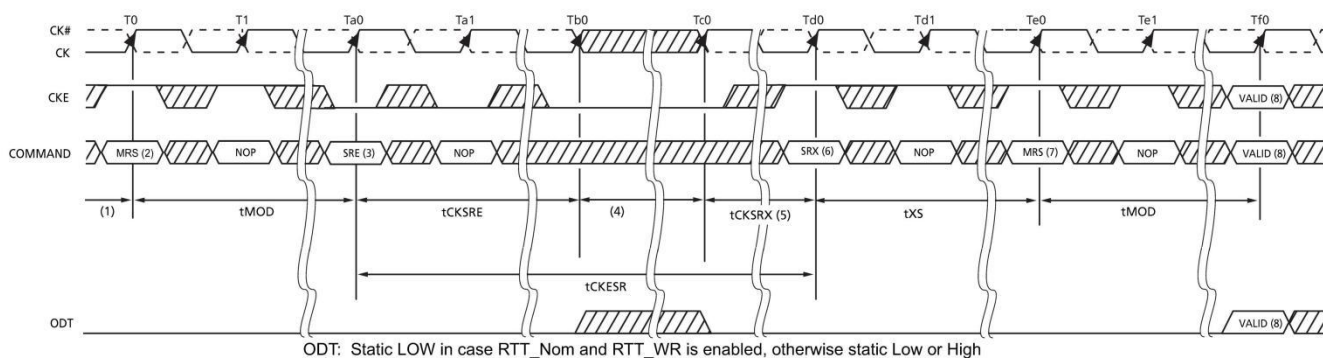
the DRAM on-die termination resistance matching RTT must be in a high-impedance state) before executing an MRS command to set MR1 to disable DLL.

2. Set mode register MR1 bit A0 to "1" to disable the DLL.
3. Wait tMOD clock cycles.
4. Enter self-refresh mode: wait to satisfy tCKSRE.
5. To change the frequency, refer to the guidance in the 'Input Clock Frequency Change' section.
6. When exiting self-refresh, the DRAM must have a stable clock for at least tCKSRX.
7. Starting from the Self Refresh Exit command, CKE must be held HIGH continuously until all tMOD timing requirements from any MRS command are satisfied. Additionally, if any ODT function is enabled in the mode register when entering self refresh mode, the ODT signal must be held LOW continuously until all tMOD timing requirements from any MRS command are satisfied. If both ODT functions are disabled in the mode register when entering self refresh mode, the ODT signal may be held LOW or HIGH.
8. After waiting tXS clocks, set the mode registers with appropriate values (especially updates to CL, CWL, and WR may be necessary).

The ZQCL command may also be issued after tXS.

9. After waiting tMOD clock cycles, the DRAM is ready for the next command.

DLL Enable to Disable Procedure Timing:



- NOTES:
1. Starting with Idle State, RTT in Hi-Z state
 2. Disable DLL by setting MR1 Bit A0 to 1
 3. Enter SR
 4. Change Frequency
 5. Clock must be stable tCKSRX
 6. Exit SR
 7. Update Mode registers with DLL off parameters setting
 8. Any valid command



TIME BREAK



DON'T CARE

Figure 11 DLL Enable/Disable Procedure Timing Diagram

5.2.4.2

DLL Disable/Enable Switching Procedure

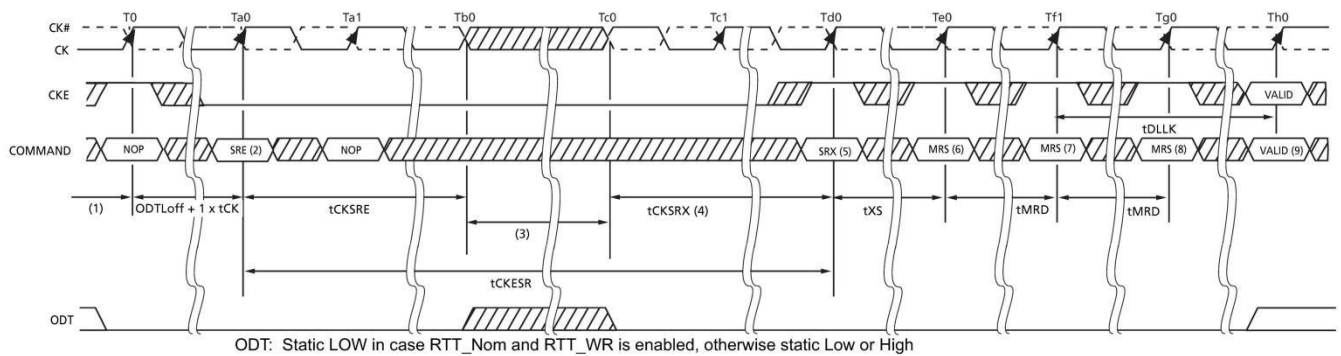
To switch from DLL "Disable" to DLL "Enable" during self refresh (frequency change required):

1. Starting from the idle state (before entering self-refresh mode, all banks must be precharged, all timing parameters satisfied, and the DRAM's on-die termination (RTT) must be in a high-impedance state).
2. Enter self-refresh mode and wait until the tCKSRE clock cycles are satisfied.

3. To change the frequency, refer to the guidance in the 'Input Clock Frequency Change' section.
4. While keeping a stable clock at the DRAM input, satisfy at least tCKSRX clock cycles.
5. Starting from the self-refresh exit command, CKE must be held continuously HIGH until the tDLLK timing requirement of the subsequent DLL Reset command is satisfied. Additionally, when entering self-refresh mode, if any ODT function is enabled in the Mode Register, the ODT signal must be held continuously LOW until the tDLLK timing requirement of the subsequent DLL Reset command is satisfied. If both ODT functions are disabled in the Mode Register when entering self-refresh mode, the ODT signal may be held either LOW or HIGH.
6. Wait tXS clock cycles, then set Mode Register MR1 bit A0 to '0' to enable the DLL.
7. Wait tMRD clock cycles, then set Mode Register MR0 bit A8 to 1 to initiate DLL Reset.
8. Wait tMRD clock cycles, then set the Mode Register with appropriate values (especially updates to CL, CWL, and WR may be necessary. After any ongoing MRS command satisfies the tMOD timing requirement, the ZQCL command may also be issued during or after tDLLK).
9. Wait tMOD clock cycles, then the DRAM is ready for the next command (before applying commands that require DLL locking, keep in mind

wait tDLLK clock cycles after DLL reset). Additionally, in the case of issuing a ZQCL command, wait tZQoper clock cycles.

DLL-off to DLL-on timing:



- NOTES:
1. Starting with Idle State
 2. Enter SR
 3. Change Frequency
 4. Clock must be stable tCKSRX
 5. Exit SR
 6. Set DLL on by MR1 A0=0
 7. Update Mode registers
 8. Any valid command

TIME BREAK DON'T CARE

Figure 12: DLL-off/DLL-on timing diagram

Input Clock Frequency Change

Once the DDR3 SDRAM is initialized, it requires the clock to be 'stable' in almost all normal operating states. This means that once the clock frequency is set and in a 'stable state', the clock period must not deviate except as allowed by clock jitter and SSC (spread-spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another in two cases: (1) self-refresh mode and (2) precharge power-down mode. Changing the clock frequency is not allowed outside these two modes.

For the first case, once the DDR3 SDRAM has successfully entered self-refresh mode and ICKSRE is satisfied, the clock state becomes 'don't care'. Once don't care, the clock frequency can be changed as long as the new clock frequency is stable before tCKSRX clock cycles. When entering and exiting self-refresh mode solely for the purpose of changing the clock frequency, the DDR3 SDRAM input clock frequency is only allowed to vary within the specified minimum and maximum operating frequencies for the given speed grade.

The second case is when the DDR3 SDRAM is in precharge power-down mode (fast exit mode or slow exit mode). If RTT_NOM is enabled in the mode register before entering precharge power-down mode, the ODT signal must be driven low continuously to ensure RTT is disabled. If RTT_NOM is disabled in the mode register before entering precharge power-down mode, RTT remains disabled. In this case, the ODT signal can be registered high or low. After CKE goes low, a minimum of tCKSRE clock cycles must be satisfied before the clock frequency can change. The DDR3 SDRAM input clock frequency is only allowed to vary within the specified minimum and maximum operating frequencies for the given speed grade. During the input clock frequency change, ODT and CKE must remain stable low. Once the input clock frequency is changed, a stable new clock must be provided to the DRAM for tCKSRX before exiting precharge power-down; after exiting precharge power-down and upon expiry of tXP clock cycles, the DLL must be reset by MRS. Depending on the new clock frequency, additional MRS commands may be issued to properly set WR, CL, and CWL, with CKE held high. During DLL re-lock, ODT must remain low and CKE must remain

remain high. After DLL lock time, the DRAM is ready to operate at the new clock frequency. Frequency Change During Precharge Power-Down

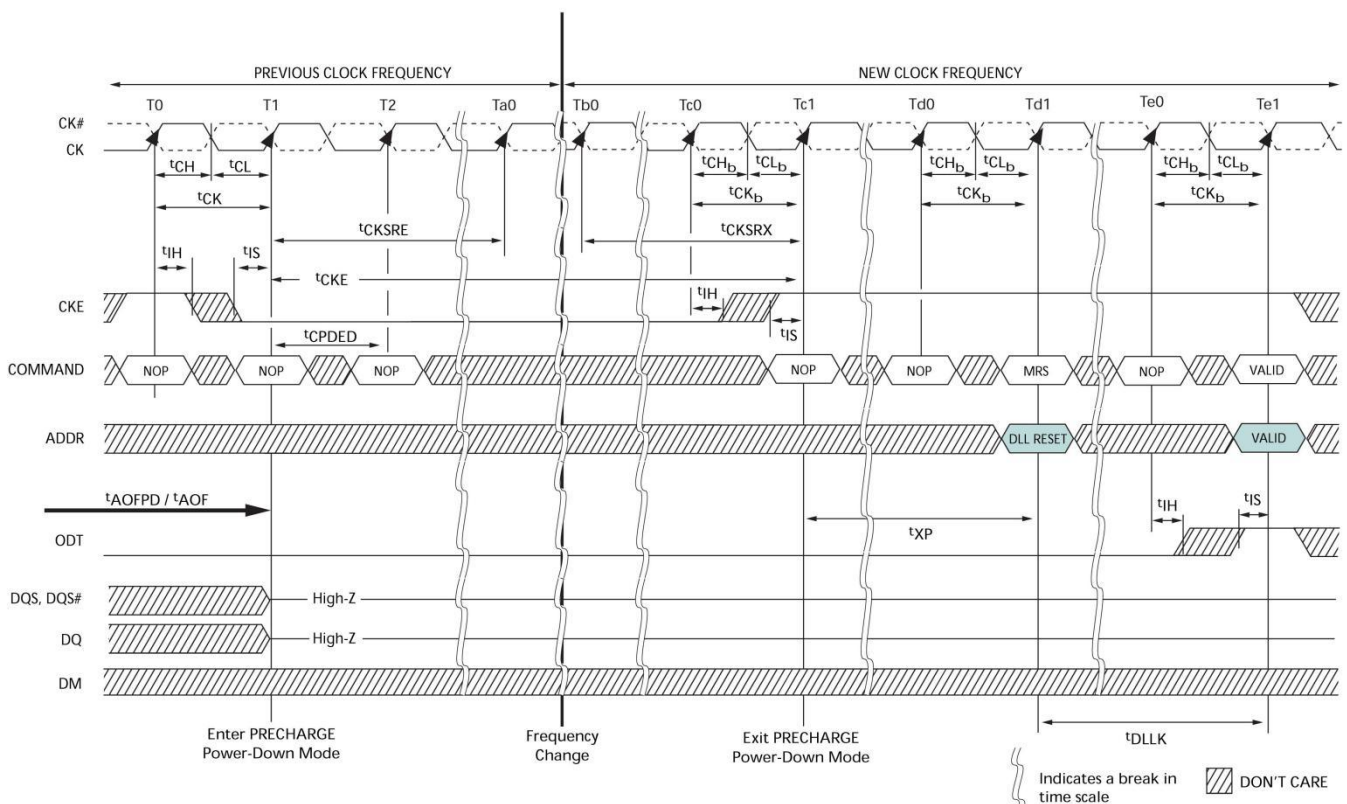


Figure 13 Mode Process Timing Diagram

Note:

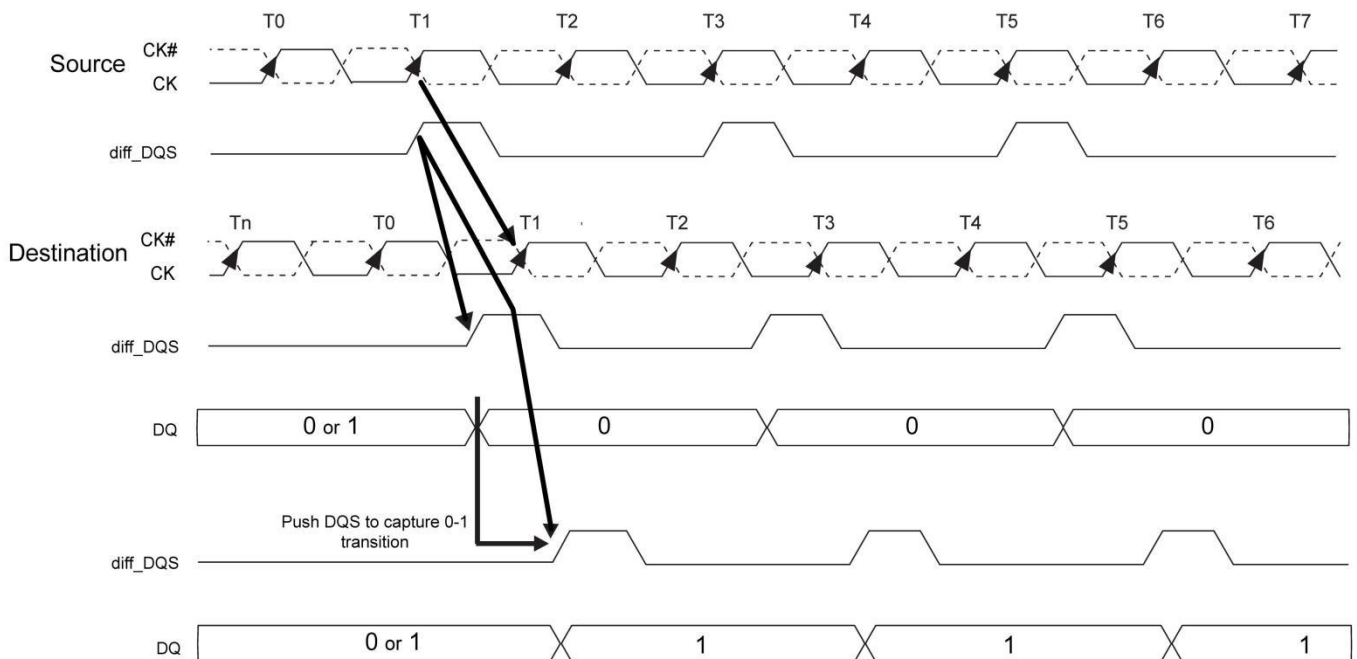
1. Applicable to Slow Exit and Fast Exit Precharge Power-Down
2. tAOPFD and tAOF timing must be satisfied, and the output must be set to high impedance before T1 timing; for specific requirements, refer to the ODT timing section.
3. If RTT_NOM is enabled in the mode register before entering precharge power-down mode, the ODT signal must be held low continuously to ensure RTT is disabled. If RTT_NOM is disabled in the mode register before entering precharge power-down mode, RTT remains disabled. In this case, the ODT signal can be held high or low.

Write Leveling

For better signal integrity, DDR3 memory adopts Fly-by topology for command, address, control signals, and clock. Fly-by topology helps reduce the number and length of stubs, but on the other hand, it causes propagation delay skew between the clock and strobe on each DRAM in the memory. This makes it difficult for the controller to maintain tDQSS, tDSS, and tDSH specifications. Therefore, the controller should support "write leveling" in DDR3 SDRAM to compensate for the skew.

The memory controller can use the write leveling function and feedback from the DDR3 SDRAM to adjust the relationship between DQS/DQS# and CK/CK#. The participating memory controller must have adjustable delay settings on DQS/DQS# to align the rising edge of DQS/DQS# with the clock rising edge at the DRAM pins. The DRAM asynchronously feeds back CK/CK# through the DQ bus, sampling the rising edge of DQS/DQS#. The controller repeatedly adjusts the delay of DQS/DQS# until a 0-to-1 transition is detected. The determined DQS/DQS# delay ensures the tDQSS specification. In addition to tDQSS, the tDSS and tDSH specifications also need to be met. One way to achieve this is to combine the actual tDQSS in the application with appropriate duty cycle and jitter on the DQS/DQS# signals. According to the actual tDQSS in the application, the actual values of tDQSL and tDQSH must be better than the absolute limits provided in "AC Timing Parameters" to satisfy the tDSS and tDSH specifications.

absolute limits provided in "AC Timing Parameters" to meet the tDSS and tDSH specifications. Write leveling timing



During leveling mode, the DQS and DQS# driven by the controller must be sampled by the DRAM. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should be configured by the DRAM to convey the leveling feedback to the controller. Therefore, it should be possible to provide, for each byte lane,✕

separate feedback mechanisms. The high-order data bits should provide feedback of the relationship between the upper diff_DQS (diff_UDQS) and the clock, while the low-order data bits similarly provide feedback for the lower diff_DQS (diff_LDQS).

5.2.4.3 DRAM Setup for Write Leveling

If A7 of Mode Register MR1 is set HIGH, the DRAM enters Write Leveling mode; after leveling is completed, if A7 is set LOW, the DRAM exits Write Leveling mode. Note that in Write Leveling mode, only DQS and DQS# terminations are enabled and disabled via the ODT pin, which differs from normal operation.

MR Settings Involved in Leveling Procedure:

Table 36 MR Settings in Leveling Procedure

Function	MR1	Enable	Disable
Write Leveling enable	A7	1	0
Output Buffer mode(Qoff)	A12	0	1

DRAM Termination Function in Write Leveling Mode:

Table 37 DRAM Termination Function in Write Leveling Mode

DRAM ODT Pin	DQS DQS# Termination	DQ Termination
De-asserted	Disabled	Disabled
Asserted	Enable	Disabled

Note:

In write leveling mode with output buffer disabled (MR1[bit7]=1, MR1[bit12]=1), all RTT_Nom settings are allowed. In write leveling mode with buffer enabled (MR1[bit7]=1, MR1[bit12]=0), only RZQ/2, RZQ/4 and RZQ/6 RTT_Nom settings are allowed.

Program Description

The memory controller initiates the leveling mode for all DRAMs by setting mode register MR1[bit7] to 1. When entering write leveling mode, the DQ pins are in an undefined drive mode. During write leveling mode, only NOP or Deselect commands are allowed, along with the MRS command to exit write leveling mode. Since the controller levels one rank at a time, the outputs of other ranks must be disabled by setting mode register MR1 A12 to 1. The controller may configure ODT after tMOD clock cycles, which is the time for the DRAM to be ready to accept the ODT signal. The controller may drive DQS low and DQS# high after a delay of tWLDQSEN clock cycles, after which the DRAM has applied termination to these signals. After tWLDQSEN and tWLMRD clock cycles, the controller provides a single DQS, DQS# edge, which is sampled by the DRAM.

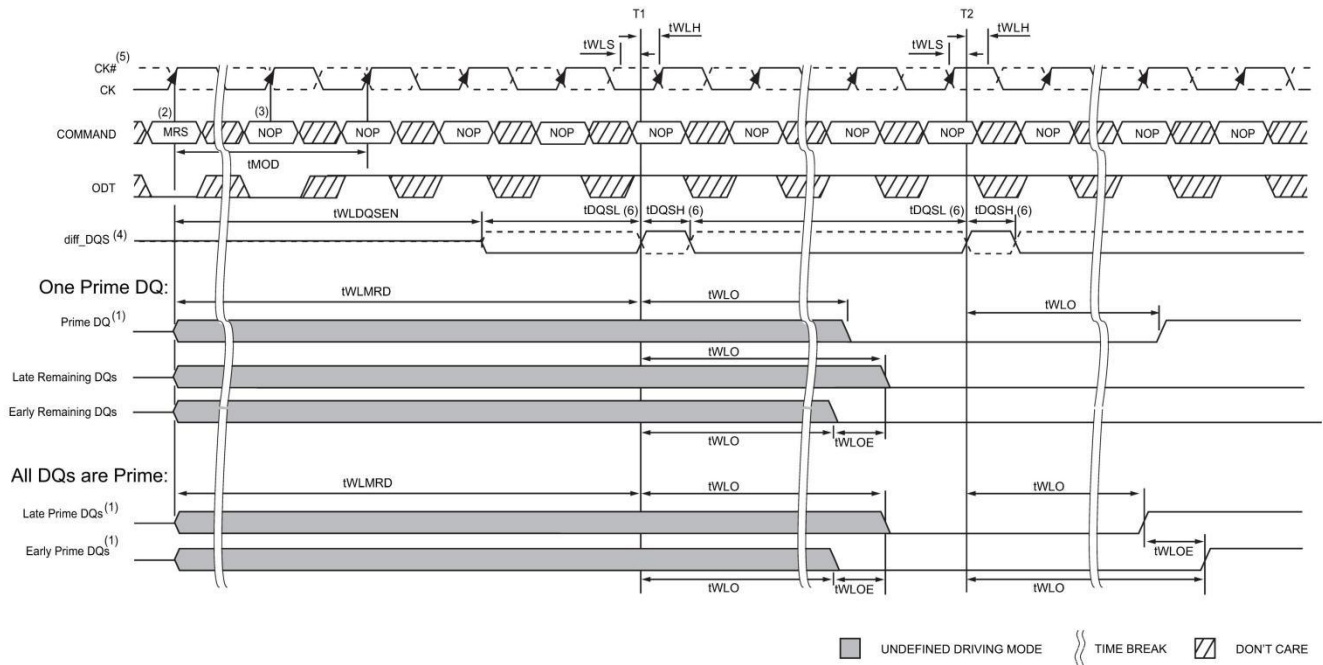
Used to sample CK/CK#. The tWLMRD (max) timing depends on the controller.

The DRAM samples the CK-CK# state using the rising edge of DQS, and after tWLO clock cycles, asynchronously provides

feedback on all DQ bits. During the t_{WLOE} clock cycles, the DQ outputs are in an undefined state, defined as allowing mismatch on the DQ bits; read strobe (DQS, DQS#)

No DQ required. The controller samples the input DQ and decides to increase or decrease the DQS-DQS# delay setting, and after a period of time initiates the next DQS, DQS# pulse, depending on the controller. Once a 0-to-1 transition is detected, the controller locks the DQS-DQS# delay setting and achieves write leveling for the device.

Timing diagram and parameters for the write leveling process. DQS-DQS# captures CK-CK# low at T1 and CK-CK# high at T2.



- NOTES: 1. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQs must be driven low, as shown in above Figure, and maintained at this state through out the leveling procedure.
2. MRS: Load MR1 to enter write leveling mode.
3. NOP: NOP or Deselect.
4. diff_DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. DQS is shown with solid line, DQS# is shown with dotted line.
5. CK, CK# : CK is shown with solid dark line, where as CK# is drawn with dotted line.
6. DQS, DQS# needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent.

Figure 15 Write Leveling Timing Diagram

Exiting Write Leveling Mode

The following sequence describes how to exit write leveling mode:

1. After the last rising strobe edge (see T0 timing), stop driving the strobe signal (see Tc0 timing). Note: From this point, the DQ pins are in an undefined drive state and will remain undefined until tMOD clock cycles after the corresponding MR command (Te1 timing).
2. Drive the ODT pin LOW (must meet tIS timing requirements) and keep it LOW (see Tb0 timing).
3. After disabling RTT, disable write leveling mode via MRS command (see Tc2 timing).
4. After tMOD clock cycles have been satisfied (Te1 timing), any valid command can be registered. (MR command can be issued after tMRD

clock cycles (Td1 timing). Write

Leveling Exit Timing

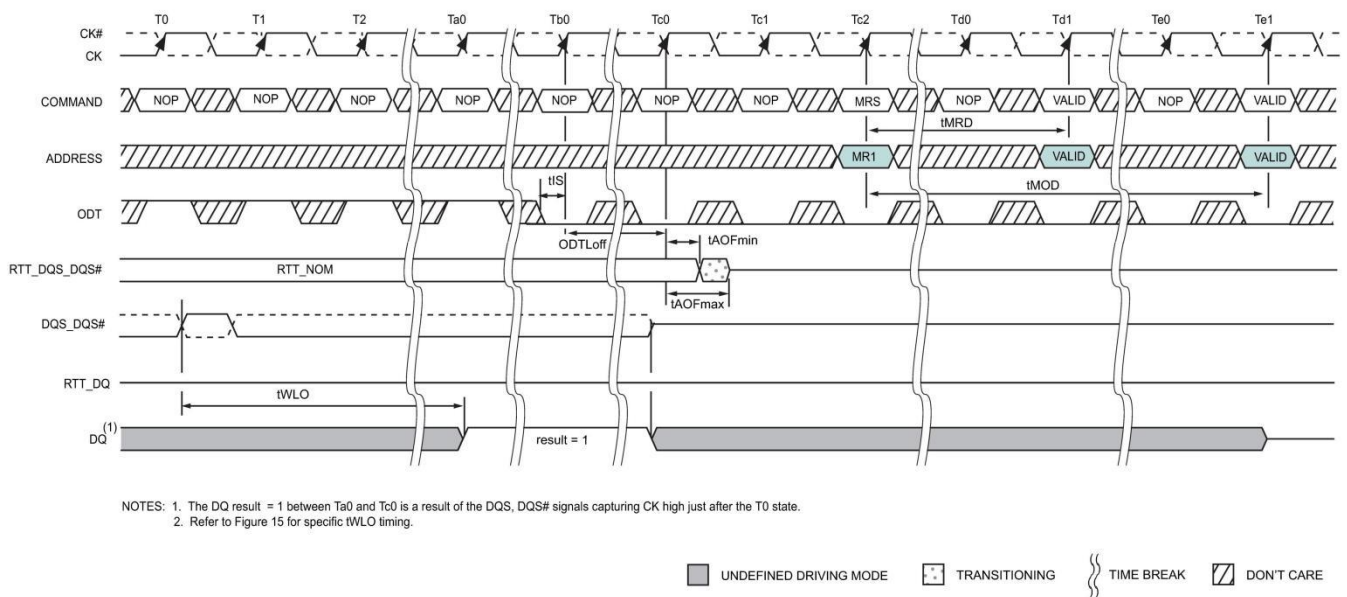


Figure 16 Write Leveling Exit Timing Diagram

Extended Temperature

DDR3 SDRAM supports an extended temperature range of -55°C to 105°C . Therefore, SRT and ASR options must be used with caution. When the case temperature exceeds $+85^{\circ}\text{C}$ (and does not exceed $+105^{\circ}\text{C}$), extended temperature range DRAM must be externally refreshed at 2 $\times$ (double refresh). The external refresh requirement is met by reducing the refresh period from 64 ms to 32 ms. Self-refresh mode requires ASR or SRT to support extended temperature. Therefore, when the temperature exceeds $+85^{\circ}\text{C}$, ASR or SRT must be enabled; self-refresh cannot be used until the case temperature is equal to or lower than $+85^{\circ}\text{C}$.

Mode Register Function Description

Table 38 Mode Register Function Description

Function Abbreviation	Function Bit	Description
ASR New	MR2 A6	Auto Self-Refresh (ASR) When enabled, the DDR3 SDRAM automatically provides self-refresh power management for all supported operating temperature values. power management function. If not enabled, the SRT bit must be programmed to ensure subsequent self- Indicates tOPER clock cycles during refresh operations. 0 = Manual SR Reference (SRT) 1 = ASR Enabled
Self Refresh Temperature Range (SRT) Temperature	MR2 A7	Self Refresh Temperature (SRT) Range: If ASR=0, the SRT bit must be programmed so that during subsequent self refresh operations indicate tOPER clock cycles. If ASR = 1, the SRT bit must be set to 0. 0 = Normal temperature range 1 = Extended temperature range

5.2.5 Auto Self-Refresh (ASR)

DDR3 SDRAM offers an auto self-refresh (ASR) mode to simplify applications. The ASR mode is enabled by setting mode register MR2 A6 = 1 and A7 = 0. The DRAM will manage the self-refresh operation in either the "normal" or "extended temperature range". In this mode, when the DRAM

operating temperature changes, the DRAM will also manage self-refresh power consumption, lower at low temperatures and higher at high temperatures. If the DRAM does not support the ASR option, the mode register MR2 A6 must be set to 0. If the ASR option is not enabled (mode register MR2 A6 = 0), then the temperature self-refresh SRT (mode register MR2 A7) must be manually programmed with the required operating temperature range during self-refresh operations. Supporting the ASR option does not automatically imply support for the extended temperature range.

5.2.6 Temperature Self-Refresh (SRT)

SRT is applicable only to devices that support the extended temperature range. If ASR = 0, the self-refresh temperature (SRT) range bit must be programmed to ensure correct self-refresh operation. If SRT = 0, the DRAM will set the appropriate refresh rate for self-refresh operation within the normal temperature range. If SRT

If the SRT bit = 1, the DRAM will set an appropriate, potentially different refresh rate to allow self-refresh operation within the normal or extended temperature range.

The value affects self-refresh power consumption; see
IDD table for details. Summary of self-refresh modes.

Table 39 Temperature Self-Refresh Mode Summary

MR2 A6	MR2 A7	Self-Refresh Operation	Allowable Operating Temperature Range for Self-Refresh Mode
0	0	Self-Refresh Rate for Normal Temperature Range	Normal
0	1	Self-Refresh for Normal or Extended Temperature Range. The DRAM must support the extended temperature range. The value of the SRT bit can affect self-refresh power consumption; see IDD table for details.	Normal Extended
1	0	Enable ASR (for devices supporting ASR and normal temperature range) Self-refresh power consumption depends on temperature.	Normal
1	1	Invalid	-

Note:

1. Normal range depends on device grade.

Industrial grade: Operating case temperature (TC) –40°C to +105° C; storage temperature (TA) –55°C to +110°C.

Wide temperature grade: Operating temperature (Tc) -40°C to 105°C; Storage temperature (Ta): -55°C to 110°C.

2. Normal and Extended ranges depend on device grade.

Industrial grade: Operating case temperature (TC) –40°C to +105° C; storage temperature (TA) –55°C to +110°C.

Wide temperature grade: Extended temperature not supported.

MR3 (MPR) Register Definition

Table 40 MR3 (MPR) Register Definition

MR3 A2	MR3 MR3A[1:0]	Function
0	Don't Care: 0/1	Normal operation, no MPR transactions. All subsequent reads will come from the DRAM Array. All subsequent writes will go to the DRAM Array.

1	1	Enable MPR mode; subsequent RD/RDA commands defined by MR3A[1:0].
---	---	---

5.2.7 MPR Register Address Definition

The following table provides an overview of the available data locations, how they are addressed by MR3A[1:0] when the MRS command writes to MR3, and how their respective bits are mapped to the burst order bits during a Multi-Purpose Register read.

Table 41 Output Data Location Overview

MR3 A2	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order Burst Order Data Pattern
1b	00b	Read system-calibrated predefined pattern	BL8	000b	Burst order: 0,1,2,3,4,5,6,7 Predefined data pattern: [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order: 0,1,2,3 Predefined data pattern: [0,1,0,1]
			BC4	100b	Burst order: 4,5,6,7 Predefined data pattern: [0,1,0,1]
1b	01b	RFU	BL8	000b	Burst order: 0,1,2,3,4,5,6,7
			BC4	000b	Burst order: 0,1,2,3
			BC4	100b	Burst order: 4,5,6,7
1b	10b	RFU	BL8	000b	Burst order: 0,1,2,3,4,5,6,7
			BC4	000b	Burst order: 0,1,2,3
			BC4	100b	Burst order: 4,5,6,7
1b	11b	RFU	BL8	000b	Burst order: 0,1,2,3,4,5,6,7
			BC4	000b	Burst order: 0,1,2,3
			BC4	100b	Burst order: 4,5,6,7

5.2.8 ACTIVATE command (ACT)

ACTIVE command is used to open (or activate) a row in a specific bank for subsequent access. The value on BA0–BA2 selects the bank, and the address provided on A0–A14 selects the row. These rows remain active (or open) for access until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

5.2.9 Precharge Command

The PRECHARGE command is used to deactivate the open row in a specific bank or the open rows in all banks. After the precharge command is issued, the specified time

(tRP), the bank will be available for subsequent row activation, except in the case of concurrent auto precharge, where read or write commands to different banks are allowed as long as they do not interrupt data transfer in the current bank and do not violate any other timing parameters. Once a bank is precharged, it is in the idle state and must be activated before any read or write command is issued to that bank. A precharge command is allowed if there is no open row in that bank (idle bank), or if the previously open row is already in the precharge process. However, the precharge cycle will be determined by the last precharge command issued to the bank.

Read Operation

5.2.9.1 Read Burst Operation

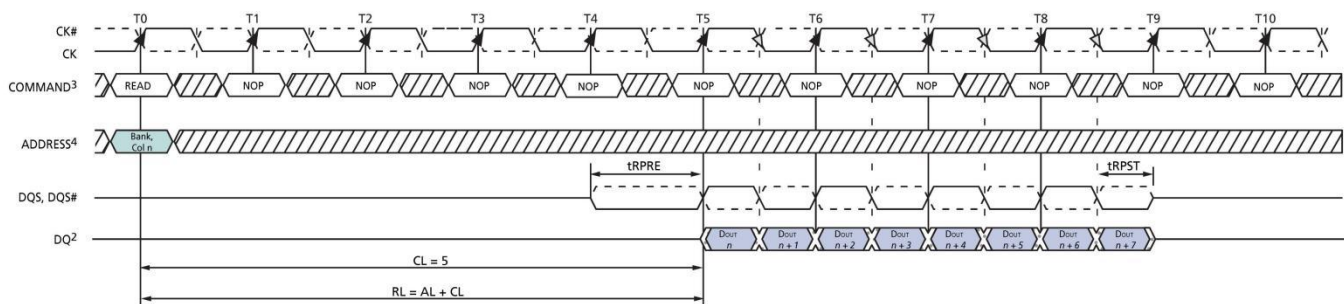
During a read or write command, DDR3 supports BC4 and BL8 modes on-the-fly by using address line A12, with auto precharge enabled or disabled during the read or write period.

A12 = 0, BC4 (BC4 = burst chop, tCCD = 4) A12 = 1,

BL8

A12 will be used only for burst length control, not column address.

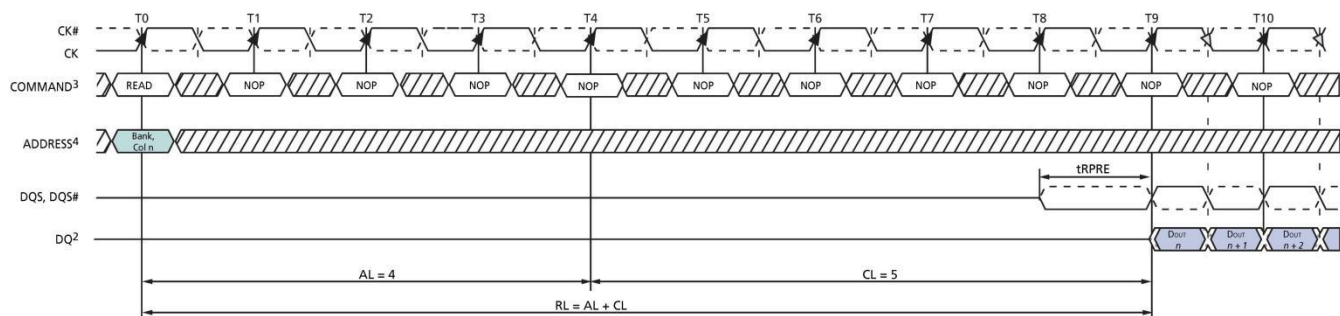
Read burst operation RL = 5 (AL = 0, CL = 5, BL = 8)



- NOTES: 1. BL8, RL = 5, AL = 0, CL = 5.
2. DOUT n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

TRANSITIONING DATA DON'T CARE

Figure 17 Read Burst Operation Timing Diagram I Read burst operation RL = 9 (AL = 4, CL = 5, BL = 8)



- NOTES: 1. BL8, RL = 9, AL = (CL - 1), CL = 5.
2. DOUT n = data-out from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

TRANSITIONING DATA DON'T CARE

Figure 18 Read Burst Operation Timing Diagram II

5.3.13.2 Read Timing Definitions

The read timing is shown in the figure below, applicable for

DLL enabled and locked state. Rising edge data strobe

parameters:

tDQSCK min/max describes the allowable range of the DQS rising edge relative to CK and /CK.

t_{DQSCK} is the actual delay of the DQS rising edge relative to CK and $/CK$.

t_{QSH} describes the DQS and $/DQS$ differential output

high time. t_{DQSQ} describes the latest valid transition

of the associated DQ pins. t_{QH} describes the earliest

invalid transition of the associated DQ pins. Falling

edge data strobe parameters:

t_{QSL} describes the DQS and $/DQS$ differential output

low time. t_{DQSQ} describes the latest valid transition

of the associated DQ pins. t_{QH} describes the earliest

invalid transition of the associated DQ pins.

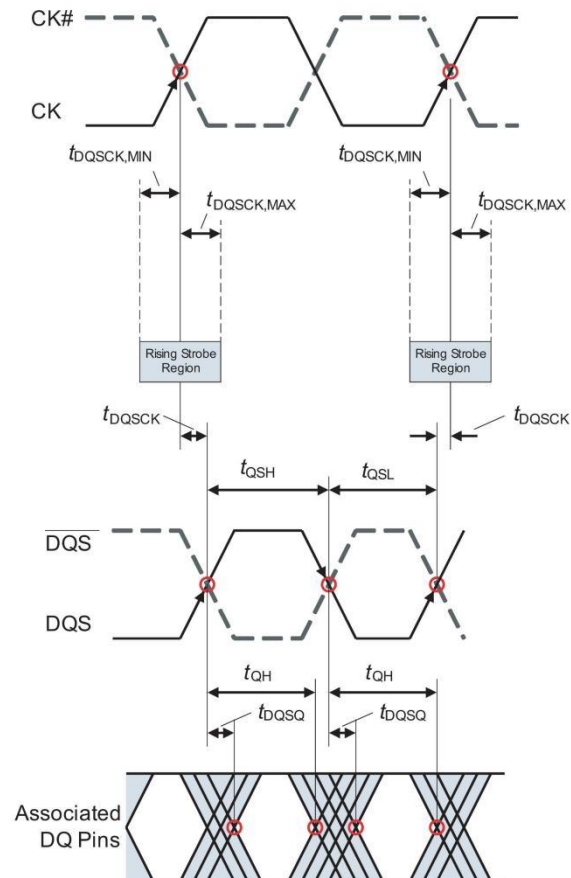


Figure 19 Read Timing Definition Process Diagram

Read Timing: Clock and Data Strobe Relationship

The relationship between clock and data strobe is shown in the figure below,

applicable when the DLL is enabled and locked. Rising edge data strobe

parameters:

t_{DQSCK} min/max describes the allowable range of the DQS rising edge relative to CK and $/CK$.

t_{DQSCK} is the actual position of the data strobe rising edge relative to CK and $CK\#$.

t_{QSH} describes the data strobe high pulse width.

Falling edge data strobe parameters:

t_{QSL} defines the data strobe low pulse width.

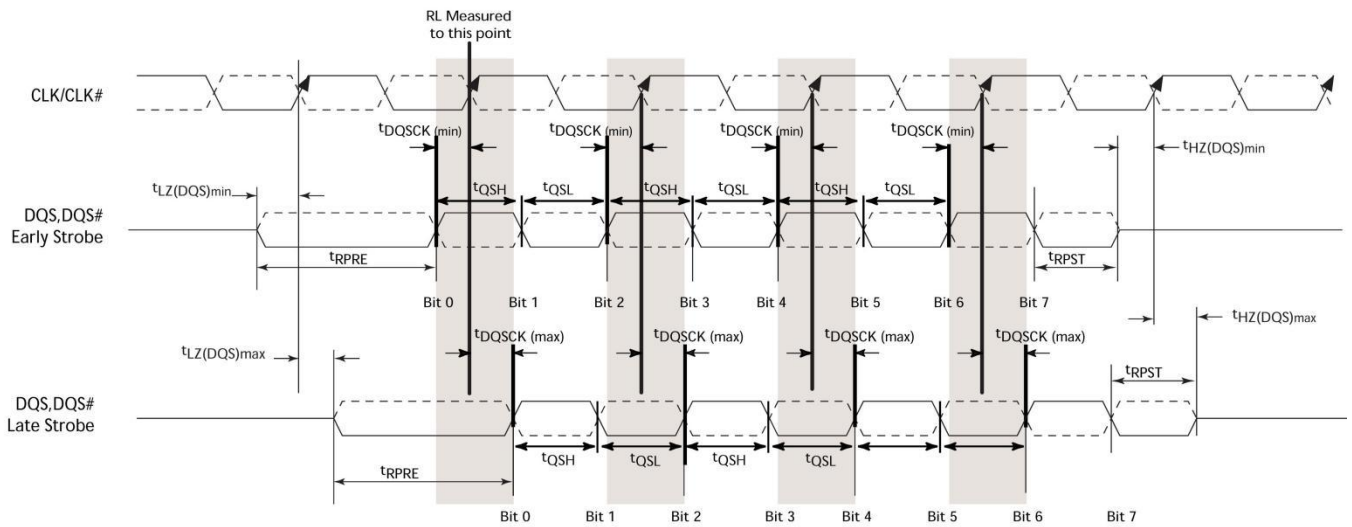


Figure 20 Clock and Data Strobe Relationship Diagram

Note:

1. During a burst, the rising edge of the data strobe is not fixed to always be at $t_{DQSK}(\min)$ or $t_{DQSK}(\max)$. Instead, the rising edge of the strobe can vary between $t_{DQSK}(\min)$ and $t_{DQSK}(\max)$.
2. The DQS, DQS# differential output high time is defined by t_{QSH} , and the DQS, DQS# differential output low time is defined by t_{QSL} .
3. Similarly, $t_{LZ}(\text{DQS})\min$ and $t_{HZ}(\text{DQS})\min$ are not bound to $t_{DQSK}\min$ (early strobe case), and $t_{LZ}(\text{DQS})\max$ and $t_{HZ}(\text{DQS})\max$ are not bound to $t_{DQSK}\max$ (late strobe case).
4. The minimum read preamble pulse width is defined by $t_{RPST}(\min)$.
5. The maximum read postamble is determined by $t_{DQSK}(\min)$ plus $t_{QSH}(\min)$ to the left of the clock and $t_{HZ}(\text{DQS})\max$ to the right of the clock.
6. The minimum read postamble pulse width is defined by $t_{RPST}(\min)$.
7. The maximum read preamble is determined by the clock edge position defined by $t_{LZDQS}(\min)$ and $t_{DQSK}(\max)$.

Read Timing: Relationship Between Data and Data Strobe

The relationship between data strobe and data is shown in the figure below, and applies when the DLL is enabled and locked. Rising edge data strobe parameters:

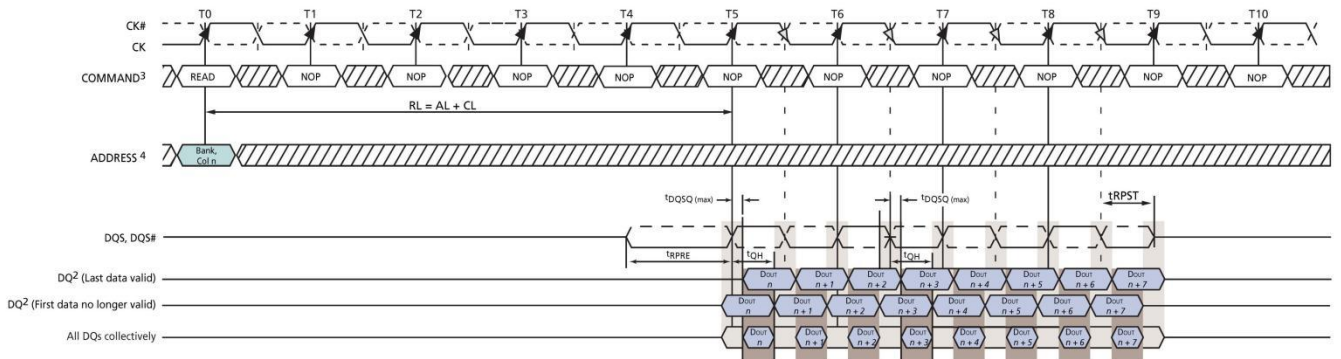
t_{DQSQ} describes the latest valid transition of the associated DQ pins.

t_{QH} describes the earliest invalid transition of the associated DQ pins. Falling edge data strobe parameters:

t_{DQSQ} describes the latest valid transition of the associated DQ pins.

t_{QH} describes the earliest invalid transition of the associated DQ pins.

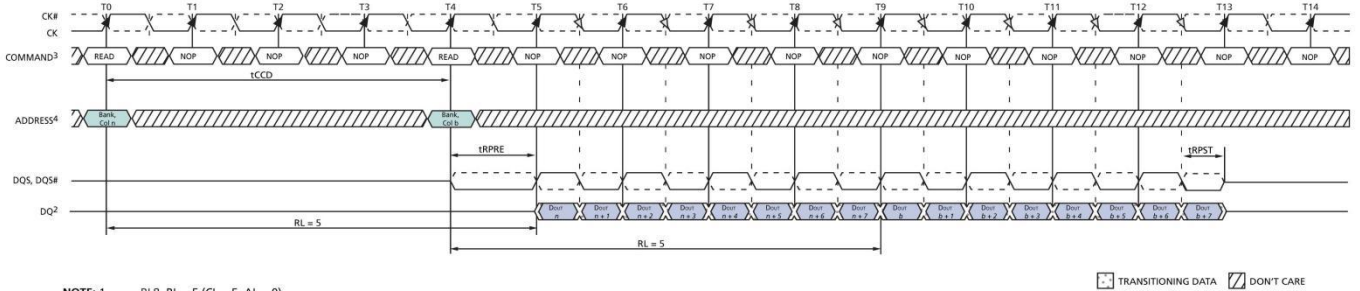
tDQSQ applies to each rising and falling edge of DQS; tAC is not defined here.



- NOTES:**
1. BL = 8, RL = 5 (AL = 0, CL = 5)
 2. Dout n = data-out from column n.
 3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
 5. Output timings are referenced to VDDQ/2, and DLL on for locking.
 6. tDQSQ defines the skew between DQS, DQS# to Data and does not define DQS, DQS# to Clock.
 7. Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

Figure 21 Data Strobe to Data Relationship Diagram

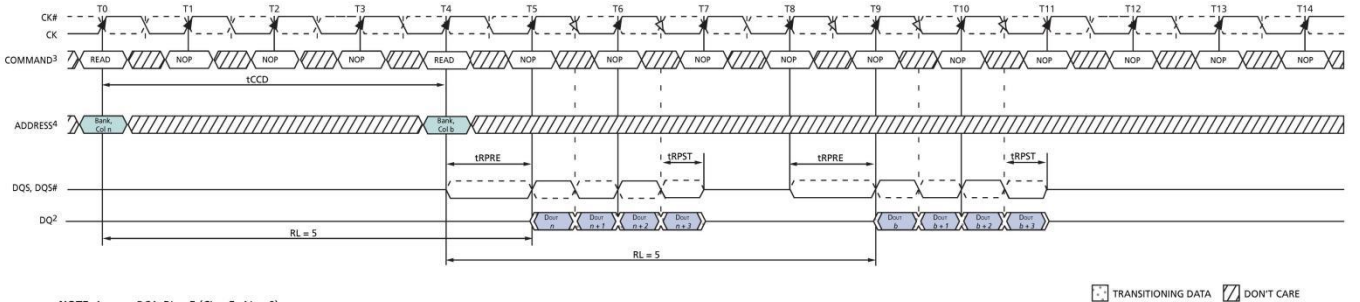
Read BL8 to Read BL8 Mode



- NOTE:**
1. BL8, RL = 5 (CL = 5, AL = 0)
 2. Dout n (or b) = data-out from column n (or column b).
 3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and T4.

Figure 22 Read BL8 to Read BL8 Mode Diagram

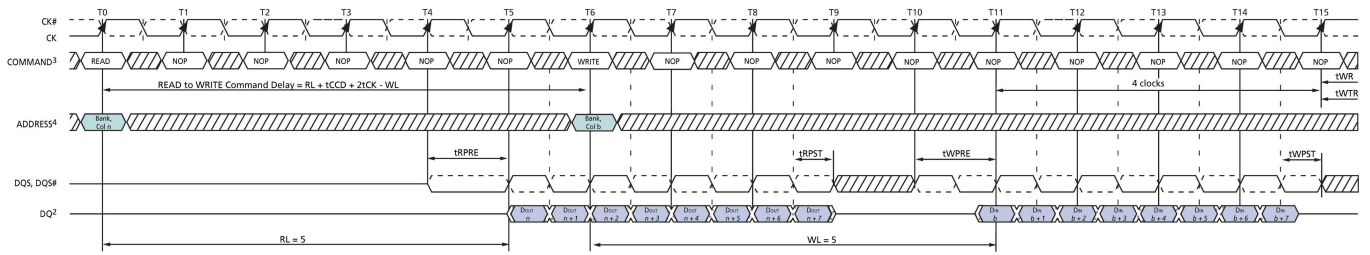
Read BC4 to Read BC4 Mode



- NOTE:**
1. BC4, RL = 5 (CL = 5, AL = 0)
 2. Dout n (or b) = data-out from column n (or column b).
 3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 4. BC4 setting activated by either MR0[A1:0 = 10] or MR0[A1:0 = 01] and A12 = 0 during READ commands at T0 and T4.

Figure 23 Read BC4 to Read BC4 Mode Diagram

Non-Consecutive Read BL8 to Read BL8 Mode



- NOTE:** 1. BL8, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
 2. DOUT n = data-out from column, DIN b = data-in from column b .
 3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 4. BL8 setting activated by either MR0[A1:0] = 00 or MR0[A1:0] = 01 and A12 = 1 during READ command at T0 and WRITE command at T6.

TRANSITIONING DATA / DON'T CARE

Figure 24 Non-Consecutive Read BL8 to Read BL8 Mode Diagram

Read BL8 to Write BL8 Mode

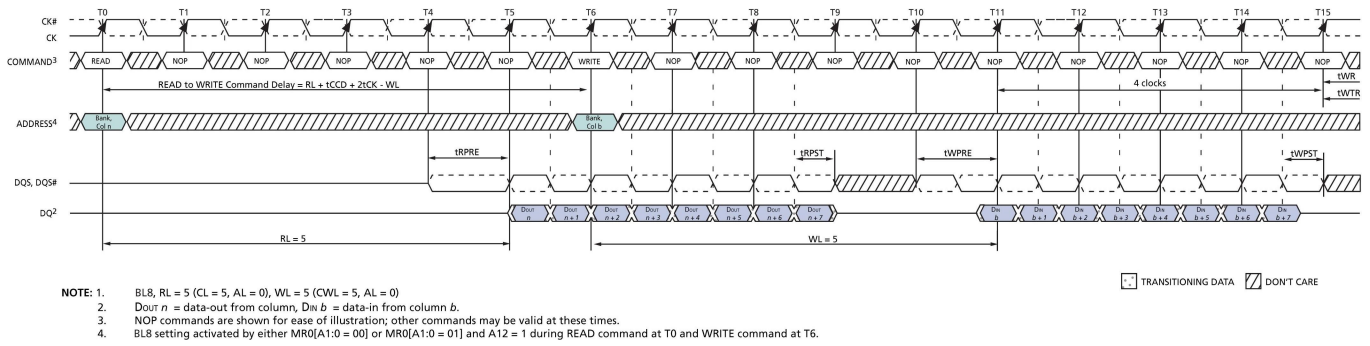


Figure 25 Read BL8 to Write BL8 Mode Diagram

Read BC4 to Write BC4 OTF Mode

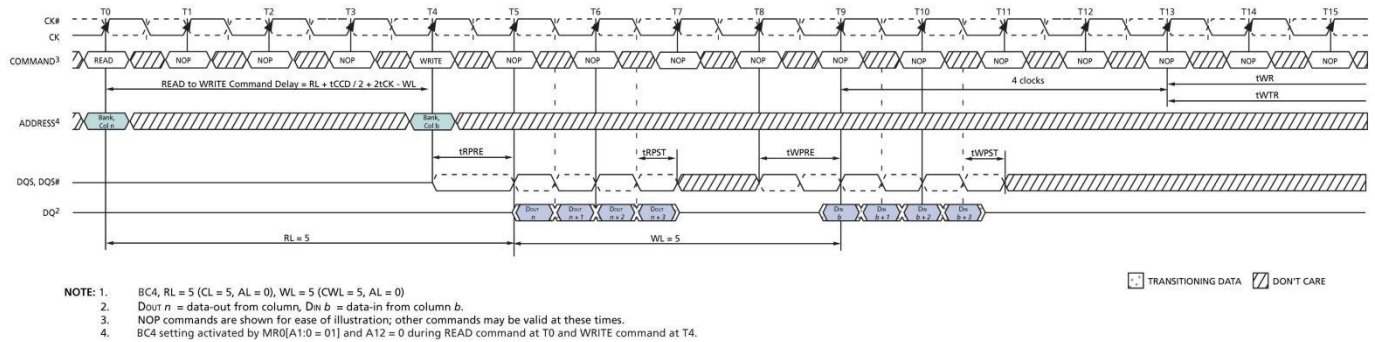


Figure 26 Read BC4 to Write BC4 (OTF Mode) – Read Precharge: RL = 8, AL = CL-2, CL = 5, tRTP = 6, tRP = 5

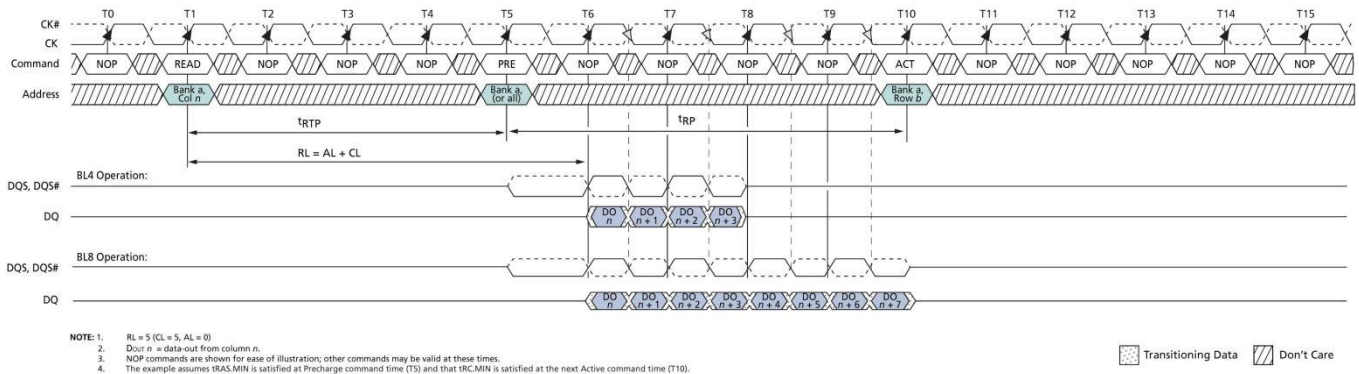


Figure 27 Read Precharge Diagram

Write Operation

5.2.9.2 DDR3 Write Burst Operation

During a read or write command, DDR3 supports BC4 and BL8 modes on-the-fly by using address line A12, with auto precharge enabled or disabled during the read or write period.

A12 = 0, BC4 (BC4 = burst chop, tCCD = 4) A12 = 1,

BL8

A12 will be used only for burst length control, not column address.

Write Timing Violation

In general, if timing parameters are violated, a full reset/initialization sequence must be initiated to ensure proper DRAM operation. However, for certain minor violations, it can be guaranteed that the DRAM will not 'hang' and the error will be limited to that specific operation.

For the following, it will be assumed that the write command itself (including ODT, etc.) has no timing conflicts and that it indeed meets all timing requirements not mentioned below.

Data Setup and Hold Time Violation

If strobe timing requirements (t_{DS} , t_{DH}) are violated for any strobe edge associated with a write burst, erroneous data may be written to the memory location addressed by the write command that violated the timing requirement.

Subsequent reads from that location may result in unpredictable read data; however, the DRAM will operate normally.
Strobe-to-Strobe, Strobe-to-Clock Violation

If the strobe timing requirements (t_{DQSH} , t_{DQSL} , t_{WPRE} , t_{WPST}) or strobe-to-clock timing requirements (t_{DSS} , t_{DSH} , t_{DQSS}) are violated for any strobe edge associated with a write burst, incorrect data may be written to the memory location addressed by the write command in question. Subsequent reads from that location may result in unpredictable read data, but the DRAM will continue to operate normally.

Write Timing Parameters

For example, this figure is only used to enumerate the strobe edges that "belong to" the write burst. Actual timing violations are not shown here. For a valid burst, all timing parameters must be satisfied for every edge of the burst (not just one edge, as shown in the figure).

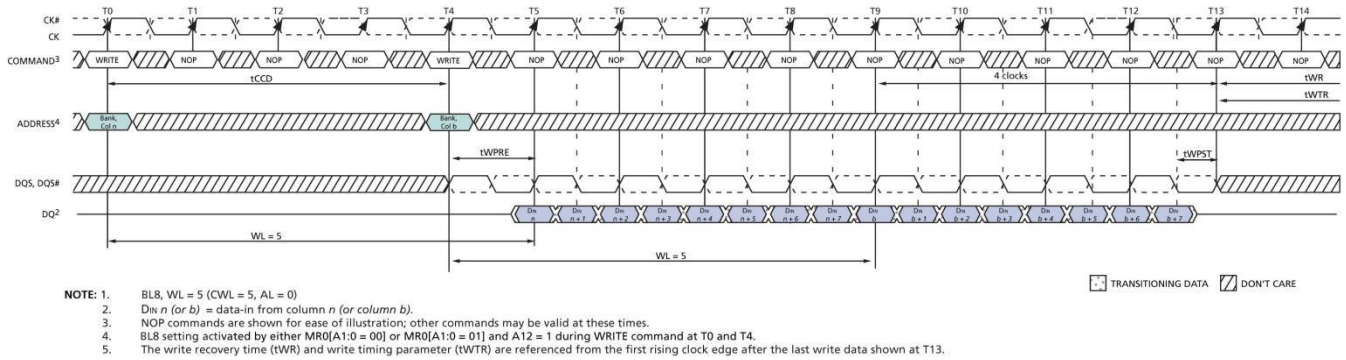


Figure 29 Write WL8 to WL8 Mode Diagram

Write BC4 to Write BC4 OTF Mode

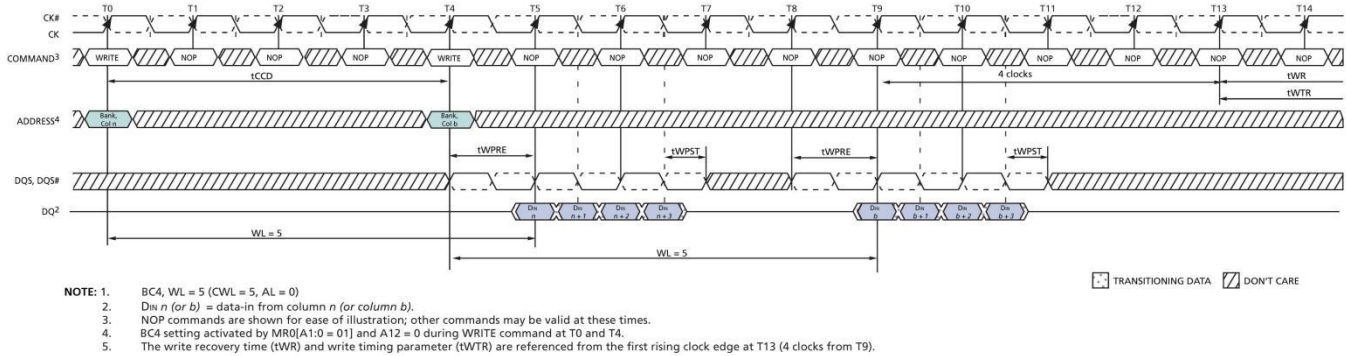


Figure 30 Write BC4 to Write BC4 OTF Mode Diagram

Write BC4 to Read BC4/BL8 OTF Mode

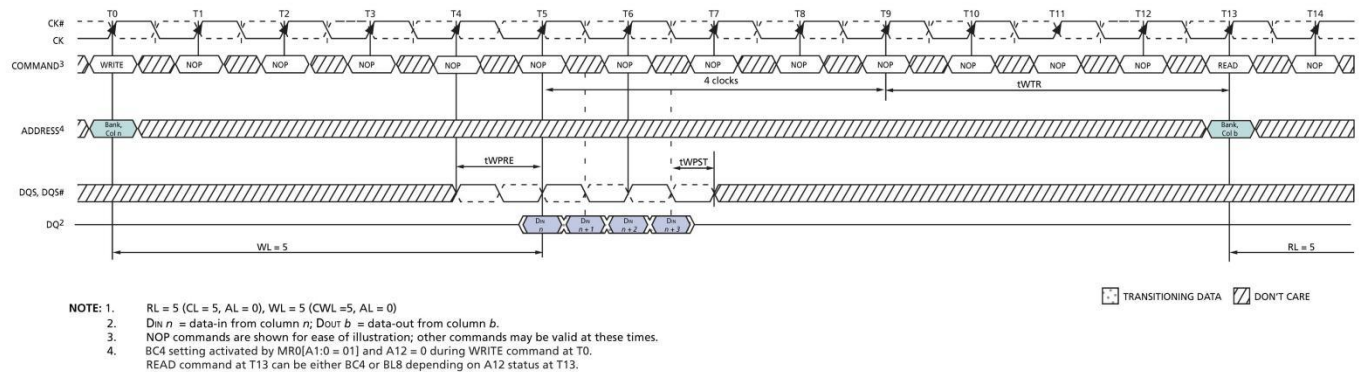


Figure 31 Write BC4 to Read BC4/BL8 OTF Mode Diagram

Write BC4 to Read BC4 Mode

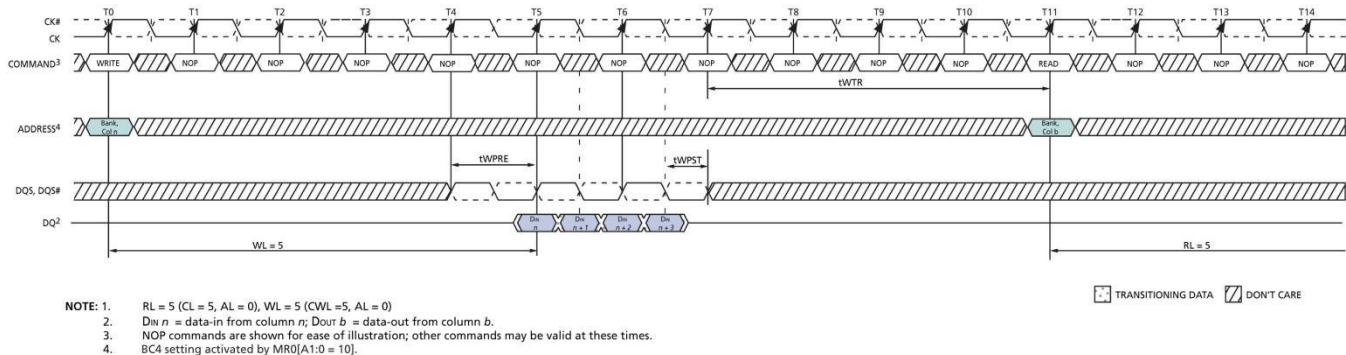


Figure 32 Write BC4 to Read BC4 Mode Diagram

Self-Refresh

The REFRESH command (REF) is used during normal operation of the DDR3 SDRAM. This command does not stop the current clock but instead causes the device to enter a refresh cycle. Before the REFRESH command can be applied, all banks of the SDRAM must be precharged and idle for at least the precharge time $t_{RP}(\text{min})$. The refresh address is generated by an internal refresh controller, making the address bits "Don't Care" during the REFRESH command. The internal address counter provides the address during the refresh cycle. Once the cycle begins, no control of the external address bus is required. When the refresh cycle completes, all banks of the SDRAM will be in the precharged (idle) state. The delay between the REFRESH command and the next valid command (except NOP or DES) must be greater than or equal to the minimum refresh cycle time $t_{RFC}(\text{min})$, as shown in the figure below.

Typically, REFRESH commands must be issued to the DDR3 SDRAM at intervals of t_{REFI} . To improve efficiency in scheduling and switching between tasks, some flexibility is provided in the absolute refresh interval.

During DDR3 SDRAM operation, up to 8 REFRESH commands can be postponed, meaning that at any point in time, a total of 8 or more REFRESH commands are not allowed. If 8 REFRESH commands are postponed consecutively, the maximum interval between adjacent REFRESH commands will be limited to $9t_{REFI}$. A maximum of $\times$

8 additional REFRESH commands may be issued early ("pull-in"), each reducing the number of required regular REFRESH commands later by one. Note that

inserting more than 8 REFRESH commands early will not further reduce the number of required regular REFRESH commands later, so the maximum interval between two surrounding REFRESH commands

is limited to $9t_{REFI}$. Before entering self-refresh mode, all pending REFRESH commands must be executed. Self-refresh entry/exit timing $\times$

Figure 33 Self-Refresh Entry/Exit Timing Diagram I

Posted Refresh Command (Example)

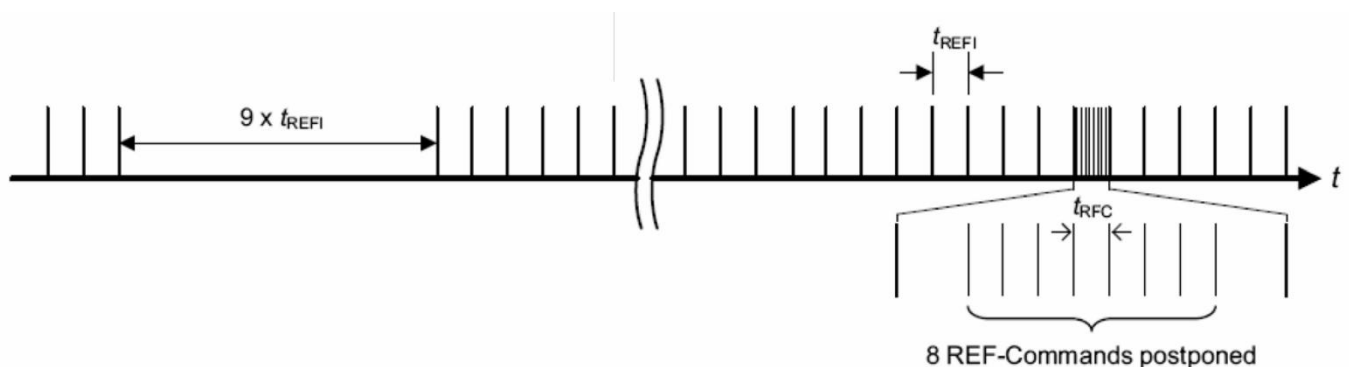


Figure 34 Posted Refresh Command Diagram

Early Refresh Command (Example)

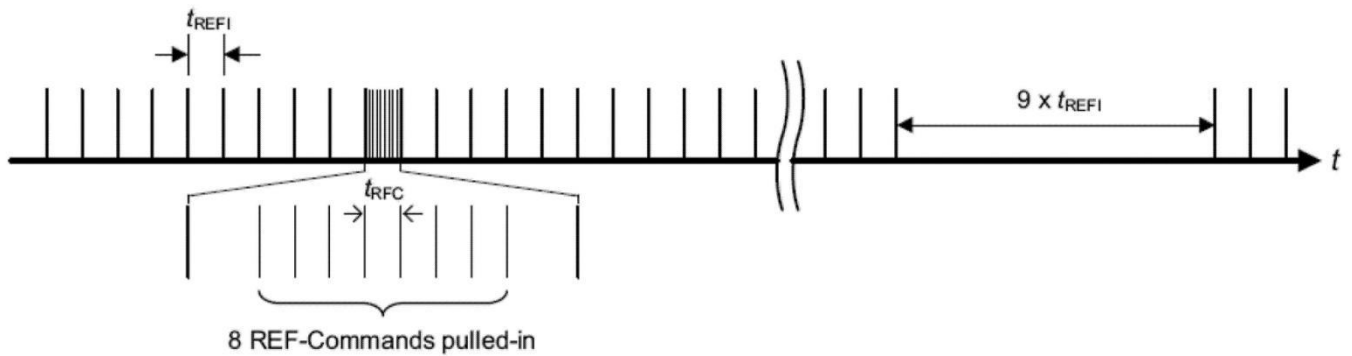


Figure 35 Early Refresh Command Diagram

Self Refresh Operation

The Self Refresh command can be used to retain data in the DDR3 SDRAM after system power-down reset. In self refresh mode, the DDR3 SDRAM retains data without an external clock. The DDR3 SDRAM controls self refresh operations via an internal timer.

Before issuing the Self Refresh Entry command, the DDR3 SDRAM must be in idle state, all banks precharged and t_{RP} satisfied. Additionally, on-die termination (ODT) must be turned off before issuing the Self Refresh Entry command, either by driving ODT LOW for at least $(ODTL + 0.5t_{CK})$ clock cycles prior to the command, or via mode register MR1 configuration. Once the Self Refresh Entry command is performed, CKE must be held LOW to place the device into self refresh mode. During normal operation (DLL enable), mode register MR1 A0=0; the DLL is automatically disabled when entering self refresh and automatically enabled (including DLL reset) when exiting self refresh.

When the DDR3 SDRAM enters self refresh mode, all external control signals except CKE and RESET# are "Don't Care". For proper self refresh operation, all power and reference pins (VDDQ, VSS, VSSQ, VRefCA, and VRefDQ) must be at valid levels. Once in self refresh mode, the DRAM initiates at least one refresh command within t_{CKE} .

During the self-refresh operation, the clock is disabled to save power. The DDR3 SDRAM must be kept at t_{CKE} for at least the self-refresh mode time. The user may change the external clock frequency or stop the external clock after entering the self-refresh command, but must satisfy t_{CKSRE} ; however, before the device exits self-refresh mode, the clock must restart and be stable for at least t_{CKSRX} time.

Exiting self-refresh mode requires a series of steps. First, the clock must be stable before CKE returns HIGH. Once a self-refresh exit command (SRX, i.e., CKE goes HIGH with a NOP or Deselect combination on the command bus) is executed, a delay of at least t_{XS} clock cycles must be satisfied before issuing a valid command that does not require DLL locking (to allow internal refresh). Before issuing commands that require DLL locking, a delay of at least t_{XSDL} clock cycles must be satisfied, and ZQCAL requirements must also be met.

Before applying commands that require DLL locking, a delay of at least t_{XSDDL} clock cycles must be satisfied. Depending on the system environment and the time spent in self-refresh, a ZQ calibration command may be needed to compensate for voltage and temperature variations as described in the "ZQ Calibration Command" section. To issue a ZQ calibration signal, the applicable timing requirements must be met.

CKE must remain HIGH for the entire self-refresh exit period t_{XSDLL} for normal operation unless re-entering self-refresh. Exiting

self-ref

After exiting self-refresh, the DDR3 SDRAM can re-enter self-refresh mode after waiting at least t_{XS} clock cycles and issuing one refresh command (refresh cycle of t_{RFC}). NOP or Deselect commands must be registered on each positive clock edge during the self-refresh exit interval t_{XS} . ODT must be disabled during t_{XSDLL} .

When using self-refresh mode, pulling CKE HIGH during self-refresh exit may cause internal refresh events to be missed.

After self-refresh, the DDR3 SDRAM requires at least one additional refresh command before re-entering self-refresh mode. Self-refresh entry/exit timing

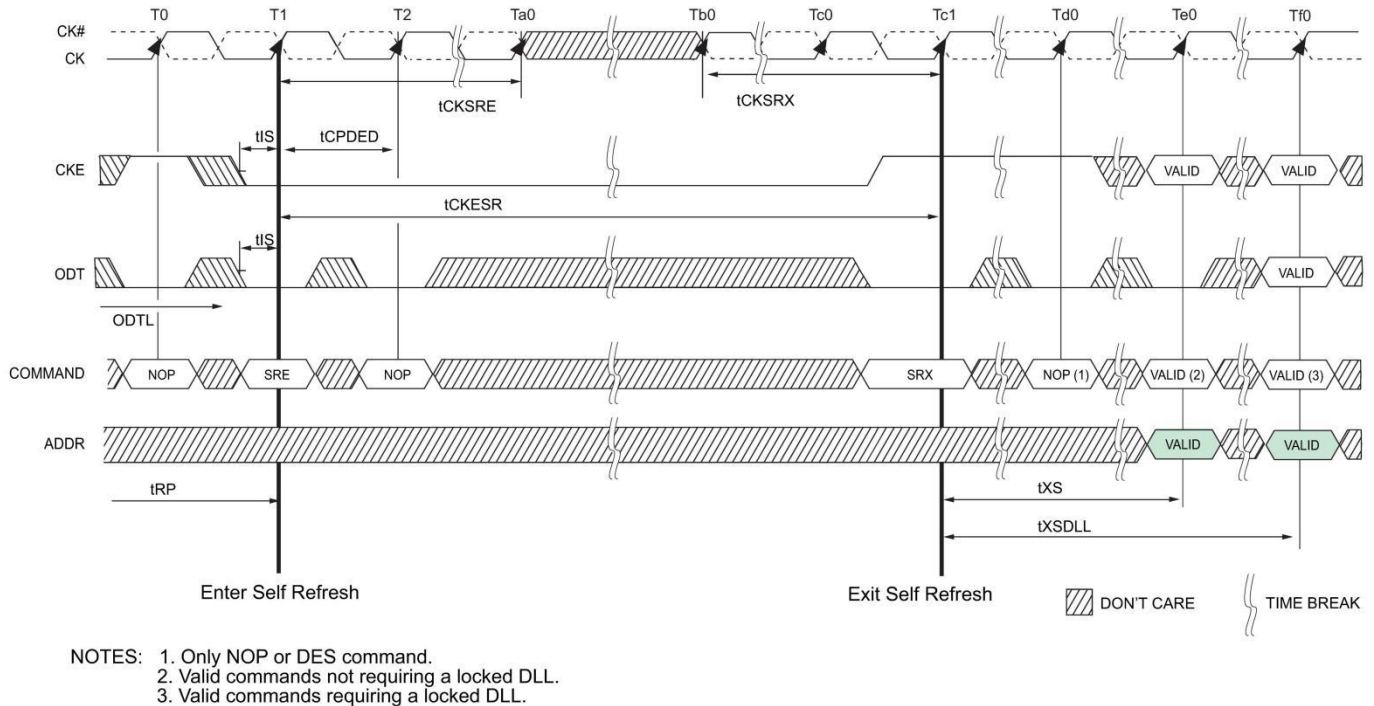


Figure 36 Self-Refresh Entry/Exit Timing Diagram II

Power-Down Mode

5.2.9.3 Entry into and Exit from Power-Down Mode

When CKE is LOW (with a NOP or Deselect command simultaneously input), the device synchronously enters power-down mode. The CKE must not be driven LOW when a mode register set command, MPR operation, ZQ calibration operation, DLL locking, or read/write operation is in progress. When any other operation (such as row activation, precharge or auto precharge, and refresh) is in progress, CKE is allowed to be LOW, but the power-down mode (IDD specification) is not applied until these operations are completed.

When entering power-down mode, the DLL should be locked to achieve the fastest power-down exit time. If the DLL is not locked at power-down entry, the DLL must be reset after exiting power-down mode for proper read operations and synchronous ODT operations. As long as the DRAM controller complies with the DRAM specification, the DRAM design provides all AC and DC timing and voltage specifications and correct DLL operation in conjunction with CKE.

During power-down, if all banks are closed after completion of any ongoing command, the device is in precharge power-down mode; if any bank is open after completion of ongoing commands, the device is in active power-down mode.

Entering power-down disables the input and output buffers, excluding CK, CK#, ODT, CKE, and RESET#. In order to protect the CKE line from

Due to the DRAM internal delays for blocking input signals, multiple NOP or Deselect commands are required during and after the CKE turn-off period. This timing period is defined as tCPDED. CKE LOW causes deactivation of the command and address receivers after tCPDED clock cycles have been satisfied.

Power-Down Entry Definition

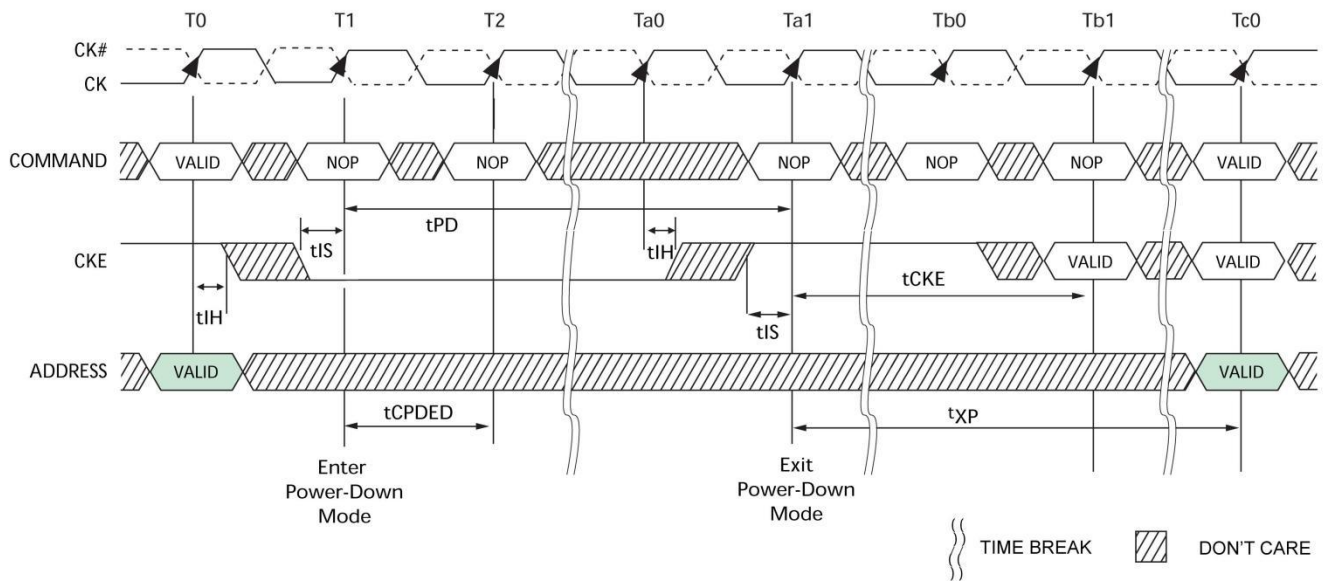
Table 42 Power-Down Entry Definition

State	MRS A12	DLL	Power-Down Exit	Related Parameter
Active (one or all banks open)	Don't Care	Enable	fast	tXP cycles for any valid command.
Precharged (all banks precharged)	0	Disabled	slow	tXP. Since in the precharged state, the commands here are ACT, AR, MRS/ERS, PR, or PREA; tXPDLL refers to commands requiring DLL operation, such as RD, RDA or ODT control commands.
Precharged (all banks precharged)	1	Enable	fast	tXP cycles for any valid command.

Additionally, the DLL is disabled when entering precharge power-down (slow-exit mode), but remains enabled in precharge power-down (fast-exit mode) or active power-down. In power-down mode, CKE is LOW, RESET# is HIGH, and a stable clock signal must be maintained at the DDR3 SDRAM inputs, ODT should be in a valid state, but all other input signals are "Don't Care" (if RESET# goes LOW during power-down, the DRAM will exit power-down and enter the reset state).

CKE LOW must be held until tCKE clock cycles are satisfied. The power-down duration is 9 times the tREFI clock cycles. When CKE is registered HIGH (along with a NOP or Deselect command), the power-down state is exited synchronously. CKE must remain HIGH until tCKE clock cycles have been satisfied. After CKE goes HIGH, valid executable commands can be applied after the power-down exit delay, tXP, and/or tXSDLL. The power-down exit delay is defined in the AC specifications table of this datasheet.

Active Power-Down Entry/Exit Timing



Note: VALID command at T0 is ACT, NOP, DES or PRE with still one bank remaining open after completion of the precharge command.

Figure 37 Active Power-Down Entry/Exit Timing Diagram

Timing diagram of CKE for power-down entry, read for power-down exit, read with auto-precharge, write with auto-precharge, activate, precharge, refresh, and MRS.

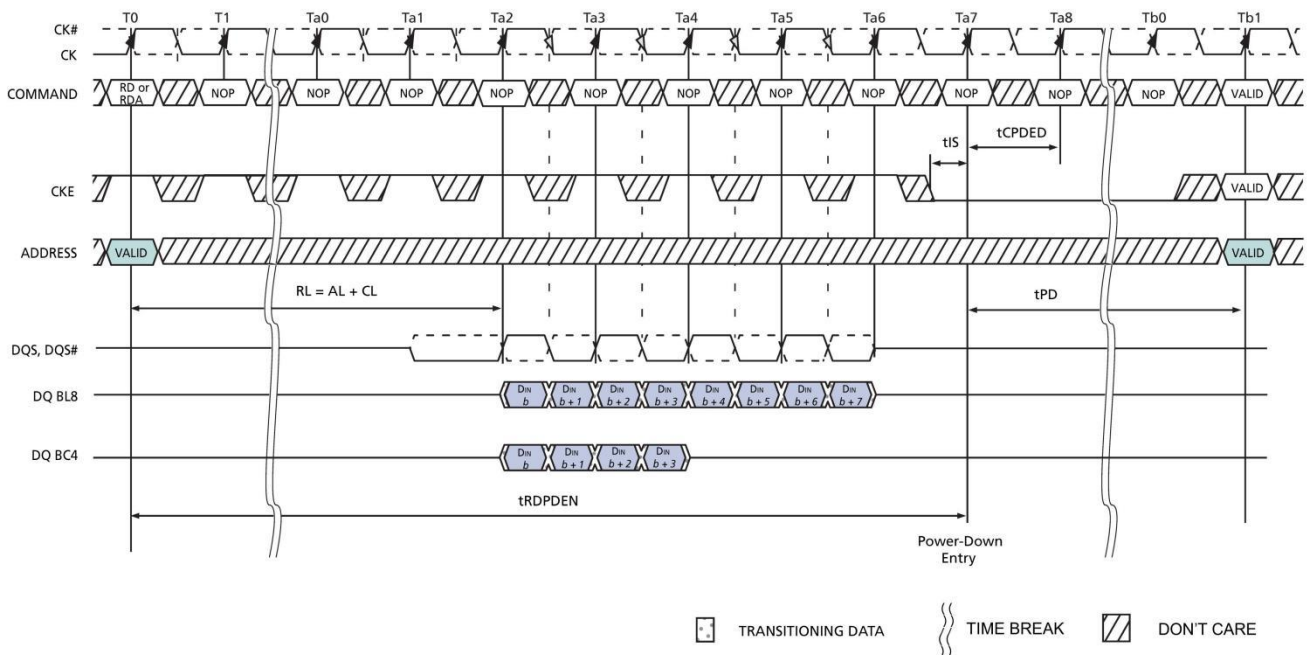


Figure 38 Power-Down Mode Timing Diagram

Power-Down after Write with Auto Precharge

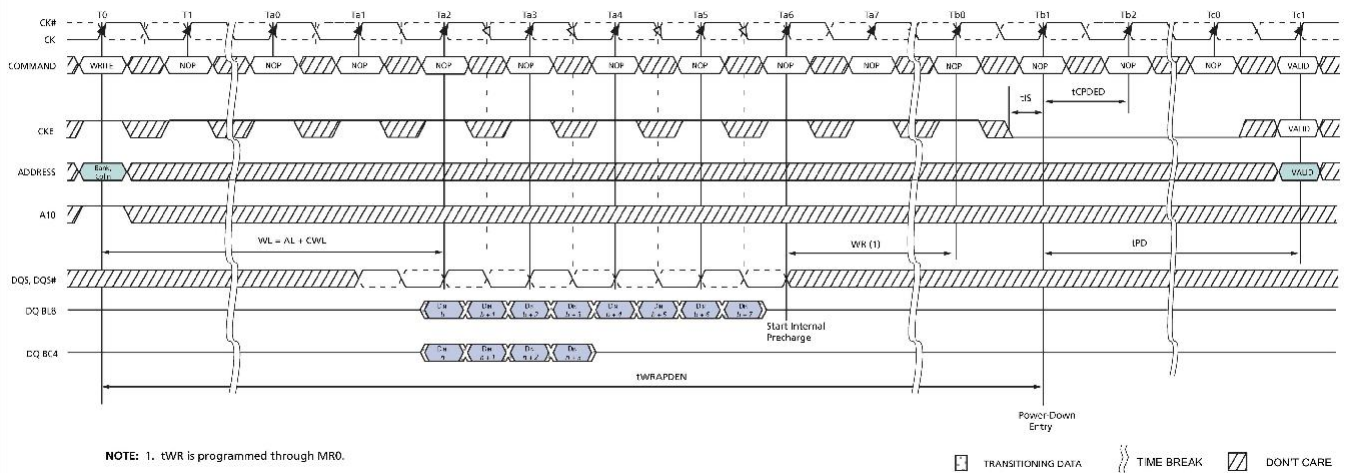


Figure 39 Auto Precharge Write Power-Down Timing Diagram

Power-Down after Write

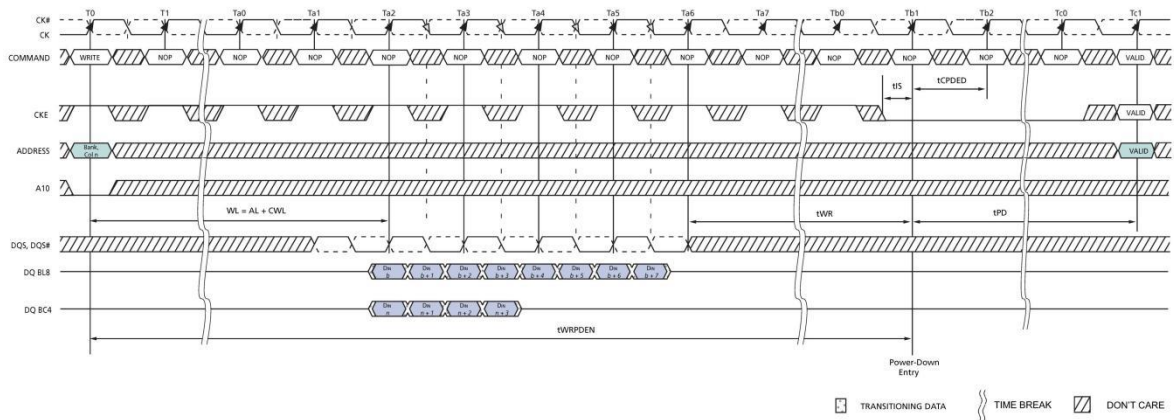


Figure 40 Power-Down after Write Timing Diagram

Precharge Power-Down (Fast-Exit Mode) Entry/Exit

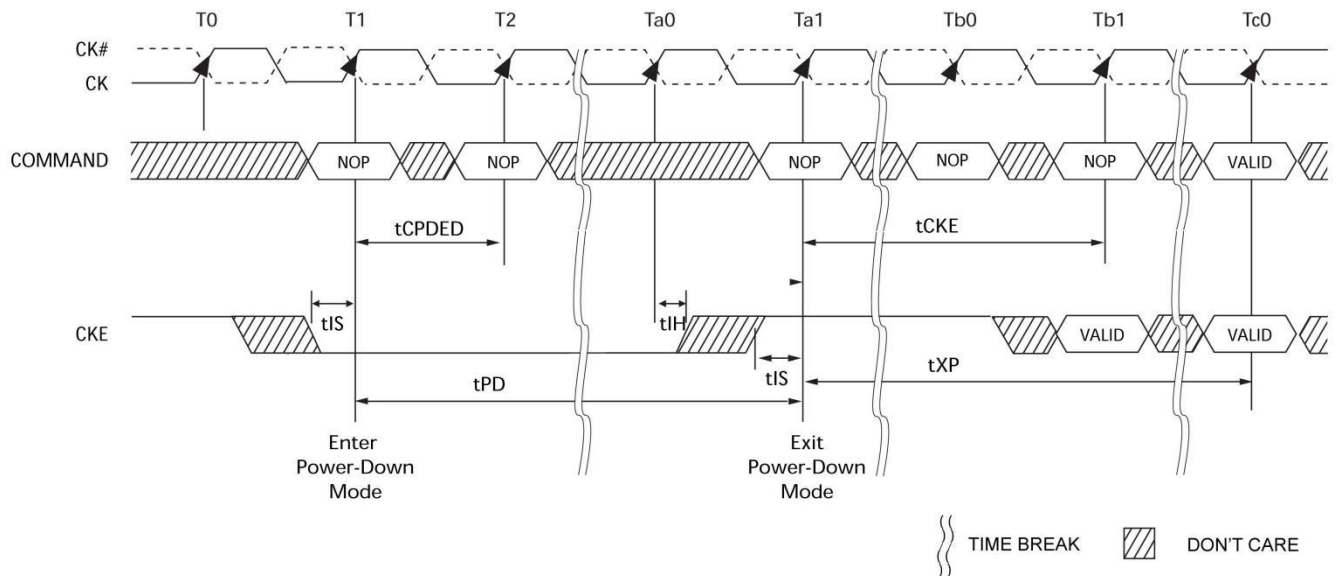


Figure 41 Fast-Exit Mode Timing Diagram

Precharge Power-Down (Slow-Exit Mode) Entry/Exit

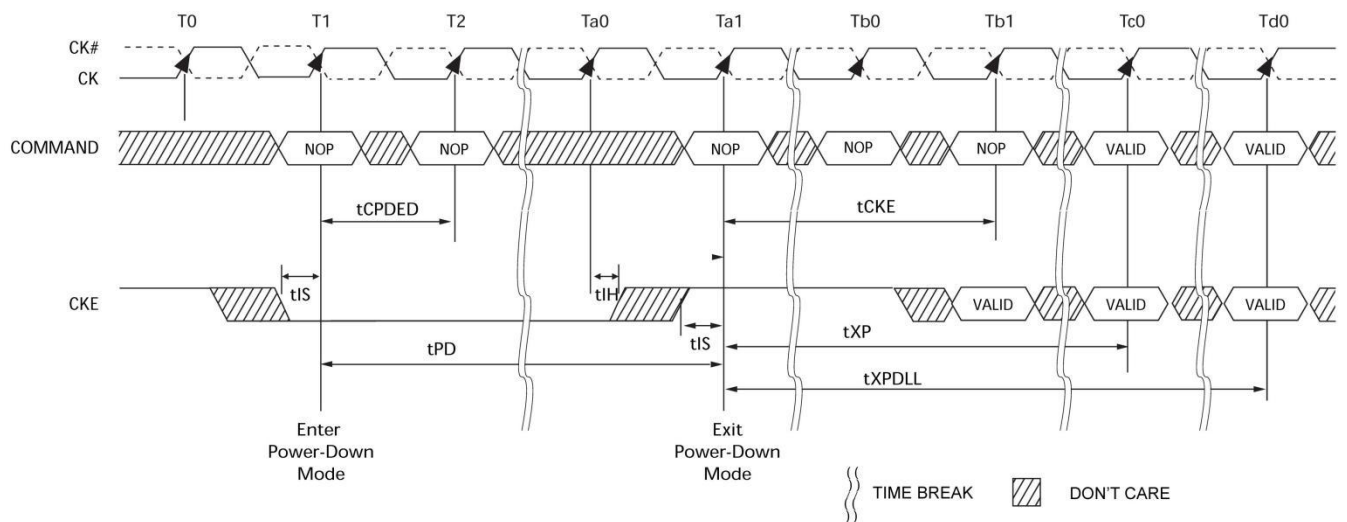


Figure 42 Slow-Exit Mode Timing Diagram

Refresh Command Power-Down Entry

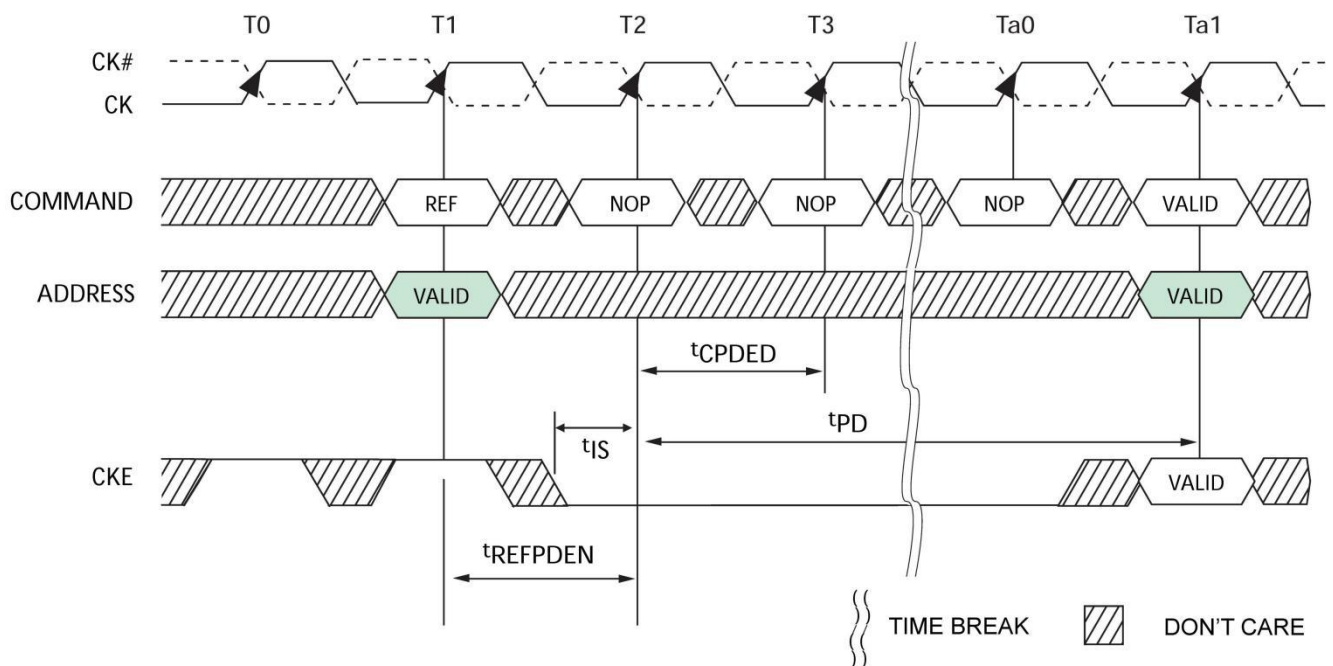


Figure 43 Refresh Command Power-Down Entry Timing Diagram

Activate Command Power-Down Entry

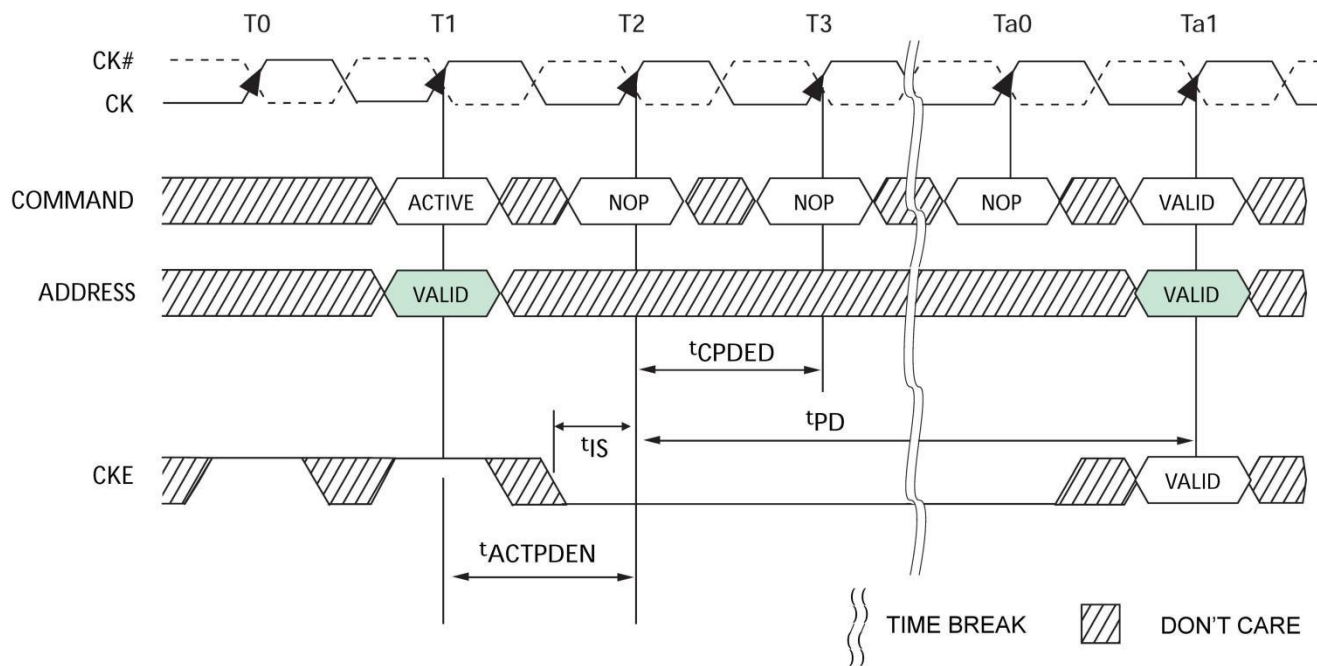


Figure 44 Activate Command Power-Down Entry Timing Diagram

Precharge/Refresh Command Power-Down Entry

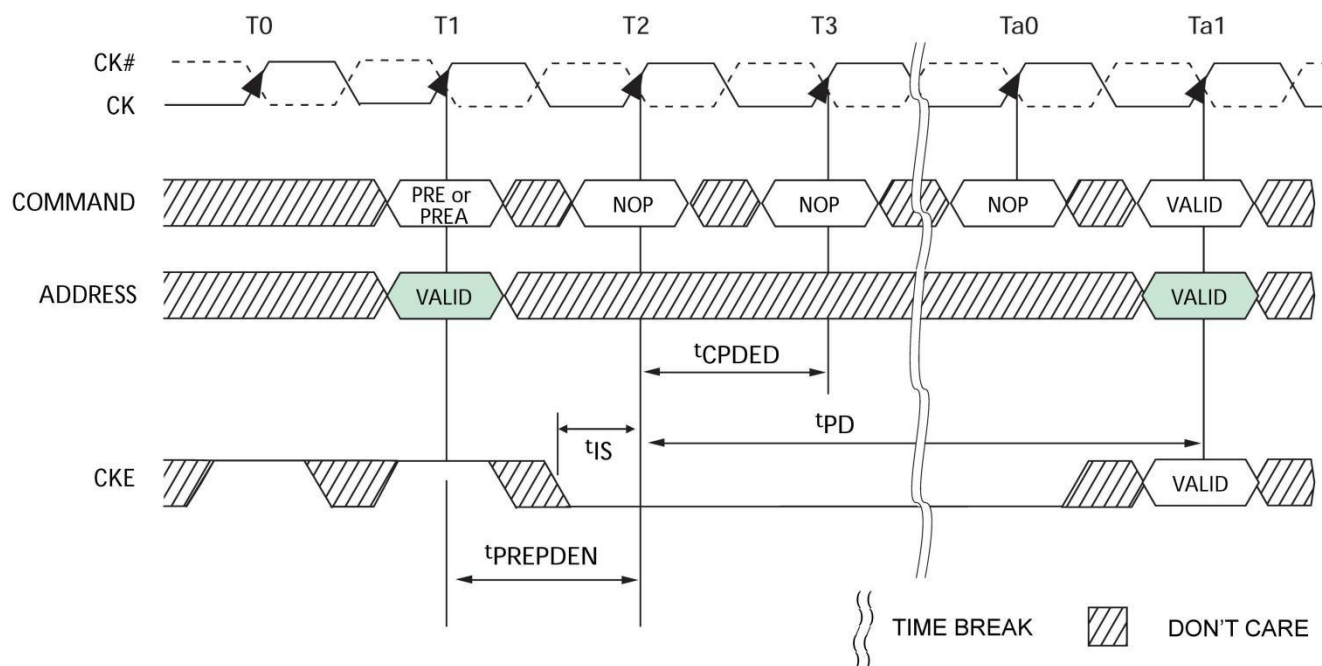


Figure 45 Precharge/Refresh Command Power-Down Entry Timing Diagram

MRS Command Power-Down Entry

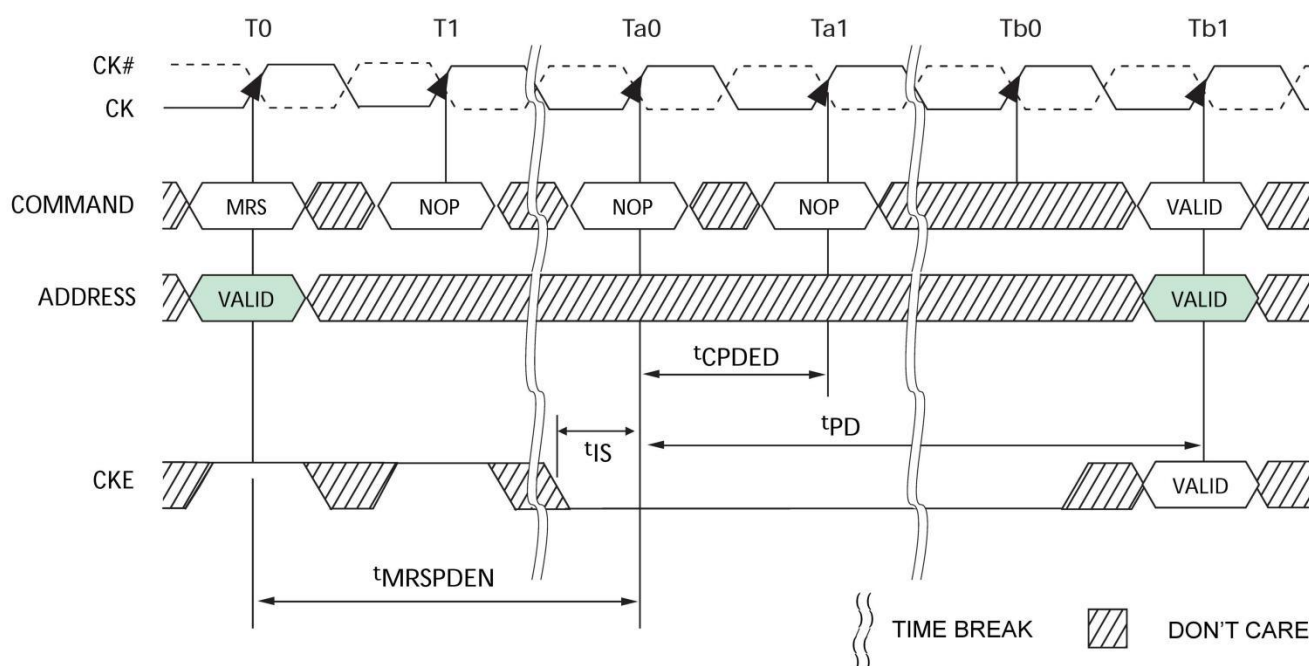


Figure 46 MRS Command Power-Down Entry Timing Diagram

5.2.10 On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of DDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, DQS#, and DM in $\times 8$ configuration, and for TDQS, TDQS# in $\times 8$, when enabled via mode register MR1 with A11 = 1. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

Resistance for any or all DRAM devices.

The ODT function is disabled and not supported in self-refresh mode. A simple functional representation of the DRAM ODT feature is shown below. Functional representation of ODT.

Figure 47 On-Die Termination (ODT) Functional Diagram

The switch is enabled by internal ODT control logic, which uses the external ODT pin and other control information. The value of RTT is determined by the setting of the mode register bits. If mode registers MR1 and MR2 are programmed to disable ODT and the device is in self-refresh mode, the ODT pin is ignored.

5.2.10.1 ODT Mode Register and Truth Table

If any of the bits in mode register MR1 (A2, A6, A9) or mode register MR2 (A9, A10) are non-zero, then ODT is enabled.

Mode. In this case, the value of RTT is determined by the settings of these bits.

Application: The controller sends a WR command together with the determined ODT.

A possible application: Provide termination for the operation of the rank being written. If the DRAM sees ODT asserted, it will turn on termination (unless ODT is disabled by MR).

The DRAM does not respond to any read or write commands.

ODT Truth Table

Table 43 ODT Truth Table

ODT Pin	DRAM Termination State
0	Disabled
1	Enabled (Disabled if Mode Register MR1 (A2, A6, A9) and Mode Register MR2 (A9, A10) are disabled))

5.2.10.2 Synchronous ODT Mode

As long as the DLL is enabled and locked, the Synchronous ODT Mode is selected. Based on the power-down mode definition, these modes are:

CKE High, Bank Active

CKE High, Refresh

CKE High, Idle Mode

Activate power-down mode (independent of mode register MR0 A12)

During precharge power-down, if DLL is enabled in precharge power-down mode, it is controlled by MR0 A12. Direct ODT function is not supported during DLL-off mode. ODT termination resistor mode is disabled and must be set through a command by keeping ODT pin low continuously and/or by programming RTT_Nom bits (mode register MR1 {A9,A6,A2} = {0,0,0}).

In synchronous ODT mode, after ODT is sampled HIGH on the rising clock edge, RTT is output after ODTLon clock cycles; and after ODT is registered LOW on the rising clock edge, it is turned off after ODTLoff clock cycles. The relationship between ODT latency and write latency (WL) is: ODTLon = WL-2; ODTLoff = WL-2.

5.2.10.3 ODT Latency and ODT Issuance

In synchronous ODT mode, the additive latency (AL) programmed into mode register MR1 also applies to the ODT signal. The delay of the internal ODT signal relative to the external ODT signal is defined by the additive latency (AL), i.e., delayed by multiple clock cycles. ODTLon = CWL+AL-2; ODTLoff = CWL+AL-2. For details, refer to the DDR3 SDRAM latency definitions.

ODT delay

Table 33 ODT Latency

Abbreviation	Parameter	DDR3-1600/1866/2133	Unit
ODTLon	ODT Turn-on Latency	WL-2 = CWL+AL-2	tCK
ODTLoff	ODT Turn-off Latency	WL-2 = CWL+AL-2	tCK

Timing Parameters

In synchronous ODT mode, the following timing parameters apply: ODTLon, ODTLoff, tAON min/max, tAOF min/max. The minimum RTT turn-on time (tAON min) is the point at which the device leaves high impedance and the ODT resistance begins to turn on. The maximum RTT turn-on time (tAON max) is the time when the ODT resistance is fully turned on. Both are measured from ODTLon. The minimum RTT turn-off time (tAOF min) is the point at which the device begins to turn off the ODT resistance. The maximum RTT turn-off time (tAOF max) is the time when the on-die termination reaches high impedance. Both are measured from ODTLoff.

When ODT is asserted, it must remain HIGH until ODT H4 is satisfied. If a write command is registered by the SDRAM while ODT is HIGH, ODT must remain HIGH until ODT H4 (for BL=4) or ODT H8 (for BL=8) after the write command. ODT H4 and ODT H8 are measured from ODT being registered HIGH to being registered LOW, or from the write command being registered to ODT being registered LOW.

Synchronous ODT Timing: AL = 3; CWL = 5; ODTLon = AL+CWL-2 = 6; ODTLoff = AL+CWL-2 = 6

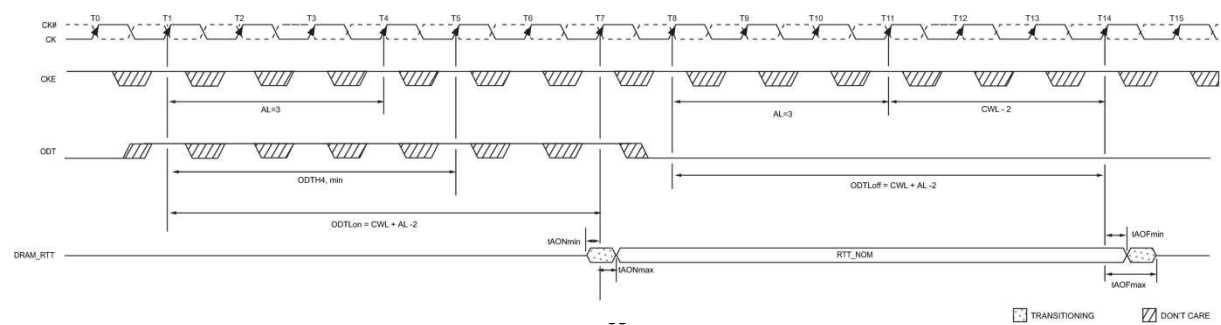


Figure 48 Synchronous ODT Mode Timing Diagram I

BL= 4;WL = 7

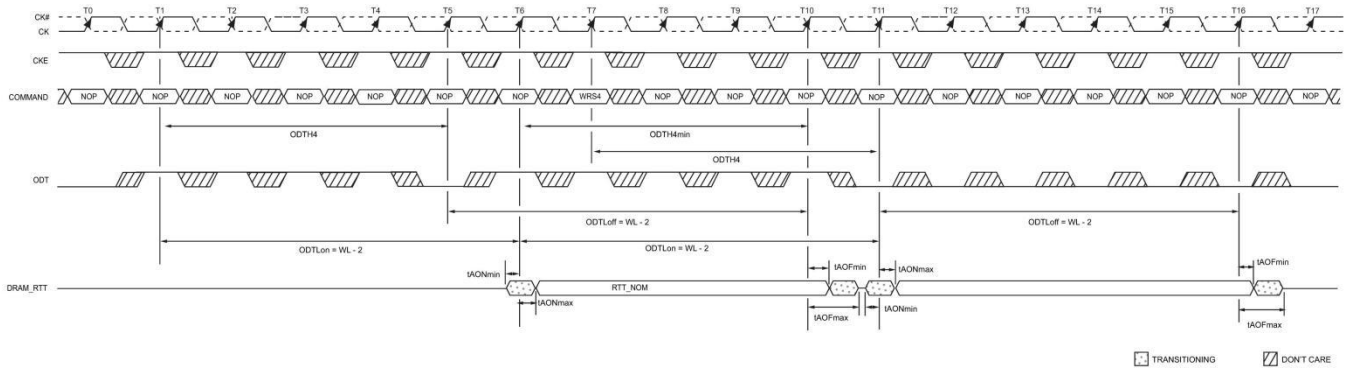


Figure 49 Synchronous ODT Mode Timing Diagram II

After assertion (T1), ODT must remain HIGH for at least ODT_{H4} clock cycles; after the write command (T7), ODT must remain HIGH for at least ODT_{H4} clock cycles.

clock cycles (BL=4) or ODT_{H8} clock cycles (BL=8).

Although the ODT registered at T6 satisfies ODT_{H4} clock cycles, ODT cannot go LOW before T11 because the ODT de-assertion for the write command at T7 must also satisfy ODT_{H4} clock cycles.

5.2.10.4 ODT During Read Operations

Because DDR3 SDRAM cannot simultaneously perform termination and driving, RTT must be disabled by pulling the ODT pin LOW appropriately at least half a clock cycle before the read preamble. RTT may not be enabled until after the postamble ends, as shown in the figure below. The DRAM turns on termination when it stops driving, which is determined by t_{HZ} clock cycles. If the DRAM stops driving early (i.e., before t_{HZ}), then the t_{AONmin} timing may apply. If the DRAM stops driving late (i.e., after t_{HZ}), then the DRAM aligns with t_{AONmax} timing. Note that ODT may be disabled before the read and enabled after the read.

During read operations, ODT must be disabled externally by driving ODT low. (Example: CL = 6; AL = CL-1 = 5; RL = AL+CL) = 11; CWL=5; ODT_{Lon} = CWL+AL-2 = 8; ODT_{Loff} = CWL+AL-2 = 8)

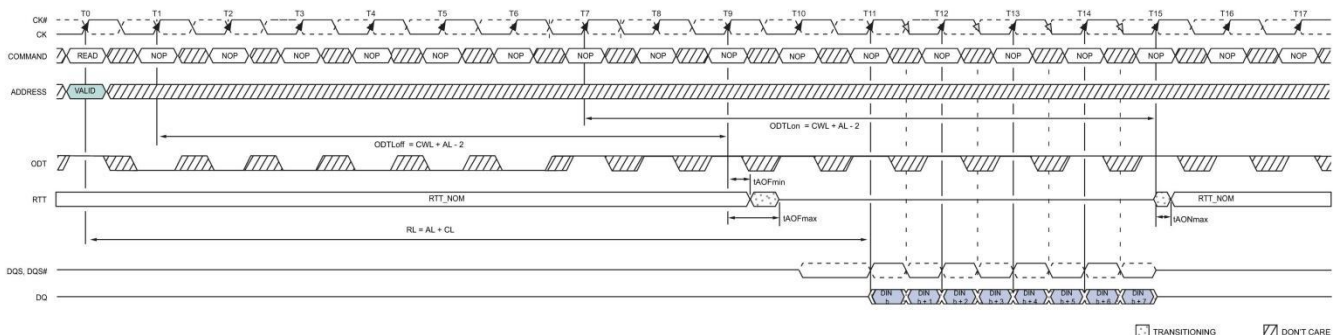


Figure 50 ODT Timing Diagram for Read Operations

5.2.10.5 Dynamic ODT

In certain applications, to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the DDR3 SDRAM without issuing an MRS command. The "Dynamic ODT" feature supports this requirement, as described

below:

Function Description

If bit A9 or A10 of mode register MR2 is set to "1", Dynamic ODT mode is enabled. The function is described as follows: Two RTT values are available: RTT_Nom and RTT_WR.

The value of RTT_Nom is pre-selected via bits A[9,6,2] in mode register MR1.

The value of RTT_WR is pre-selected via bits A[10,9] in mode register MR2.

During operations without a write command, the termination is driven as follows:

The nominal termination resistance RTT_Nom is selected.

The on/off timing of termination is controlled through the ODT pin and the delay parameters ODTLon and ODTLoff.

When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, if dynamic ODT is enabled, the termination control is as follows:

After a write command is registered, following a delay of ODTLcnw clock cycles, the termination resistor RTT_WR is selected.

After a read command is registered, following a delay of ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) clock cycles, the termination resistor RTT_Nom is selected.

The on/off timing of termination is controlled through the ODT pin and ODTLon, ODTLoff.

The following table shows the delay and timing parameters related to on-die termination control in dynamic ODT mode.

Dynamic ODT function is not supported in DLL-off mode; the user must disable external dynamic ODT by setting bits A10 and A9 of MR2 to 0,0 via an MRS command.

When ODT is pulled high, it must remain high until the ODT4 clock cycle is satisfied. If the SDRAM registers a write command while ODT is high, ODT must remain high until ODT4 clock cycles (BL=4) or ODT8 clock cycles (BL=8) after the write command. ODT4 and ODT8 are the number of clock cycles from ODT being pulled high to ODT being pulled low, or from a write command being registered to ODT being pulled low.

Low-Power Measurements

Dynamic ODT Latency and Timing Parameters

Table 34: Dynamic ODT Latency and Timing Parameters Information

Name and Description	Abbreviation	Defined from	Defined to	All DDR3 Pin Speed Definitions Pin Speed Definition	Unit
ODT Turn-On Latency	ODTLon	registering external ODT signal high	termination on	ODTLon = WL-2	tCK
ODT off delay	ODTLoff	registering external	termination off	ODTLoff = WL-2	tCK
ODT delay from RTT_Nom to RTT_WR ODT delay	ODTLcnw	registering external write command	Change RTT strength from RTT_Nom to	ODTLcnw = WL-2	tCK

			RTT_WR		
ODT delay from RTT_WR to RTT_Nom (BL=4) (BL=4) ODT delay	ODTLcnw4	registering external write command	Change RTT strength from RTT_WR to RTT_Nom	ODTLcnw4 = 4+ODTLoff	tCK
Change RTT strength from RTT_WR to RTT_Nom (BL=8) ODT delay	ODTLcnw8	registering external write command change	Change RTT strength from RTT_WR to RTT_Nom	ODTLcnw8 = 6+ODTLoff	tCK(avg)
after ODT is determined minimum time for ODT to reach high level	ODTH4	ODT registered high	ODT registered low	ODTH4 = 4	tCK(avg)
after a write command (BL=4) is determined, the minimum time for ODT to reach high level minimum time	ODTH4	write ODT registered high	ODT registered low	ODTH4 = 4	tCK(avg)
after a write command (BL=8) is determined, the minimum time for ODT to reach high level Short Time	ODTH8	registering write ODT high	ODT registered low	ODTH8 = 6	tCK(avg)
RTT Change Jitter	tADC	tDAC	RTT valid	tDAC(min) = 0.3 tCK(avg) tDAC(max) = 0.7 tCK(avg)	tCK(avg)

Note: tAOF,nom and tADC,nom are 0.5tCK (effectively adding half a clock cycle to ODTLoff, ODTcnw, and ODTLcwn)

5.2.10.6 ODT Timing

Dynamic ODT: ODT Assertion Behavior Before and After Write

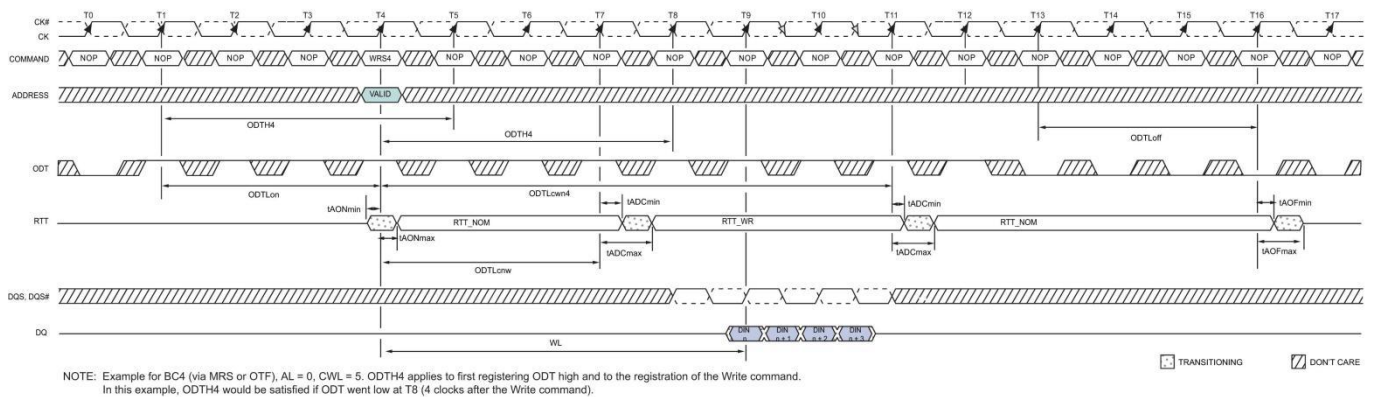


Figure 51 Dynamic ODT (ODT Assertion Before and After Write) Timing Diagram: Dynamic ODT Behavior Without Write Command, AL=0, CWL=5

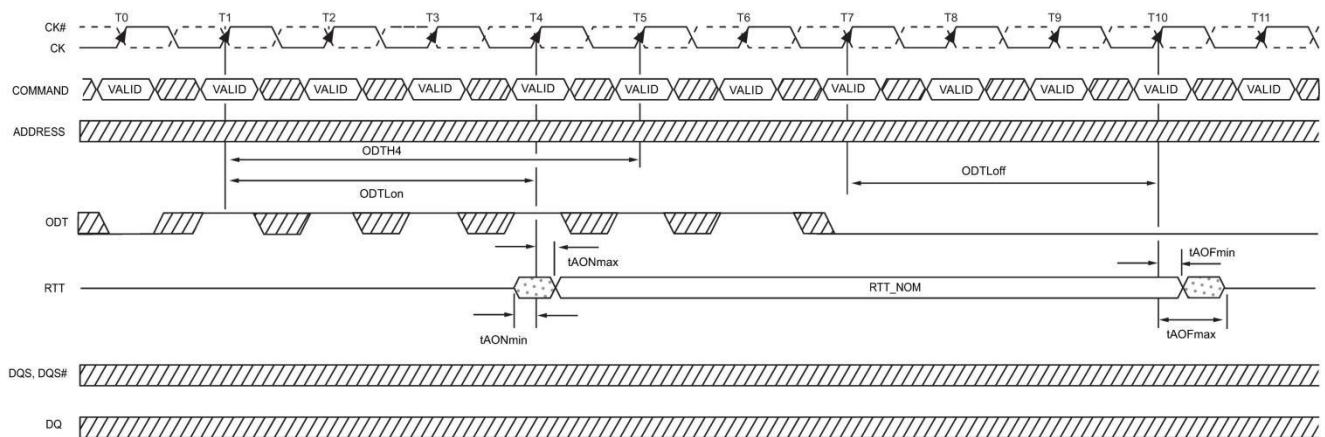


Figure 52 Dynamic ODT (Behavior Without Write Command) Timing Diagram: ODT Assertion Behavior When ODT Pin is Asserted Together with Write Command for 6 Clock Cycles

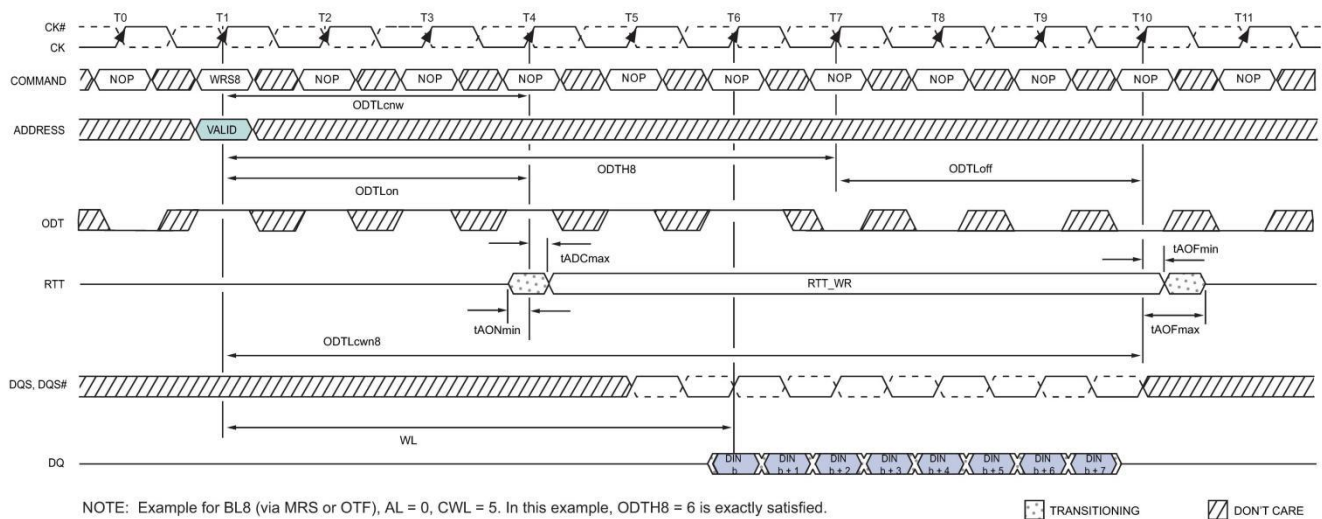


Figure 53 Dynamic ODT (Pin Assertion with Write Command) Timing Diagram I

Dynamic ODT: ODT pin asserted together with a write command for a duration of 6 clock cycles, such as BC4 (via MRS or OTF), AL=0, CWL=5

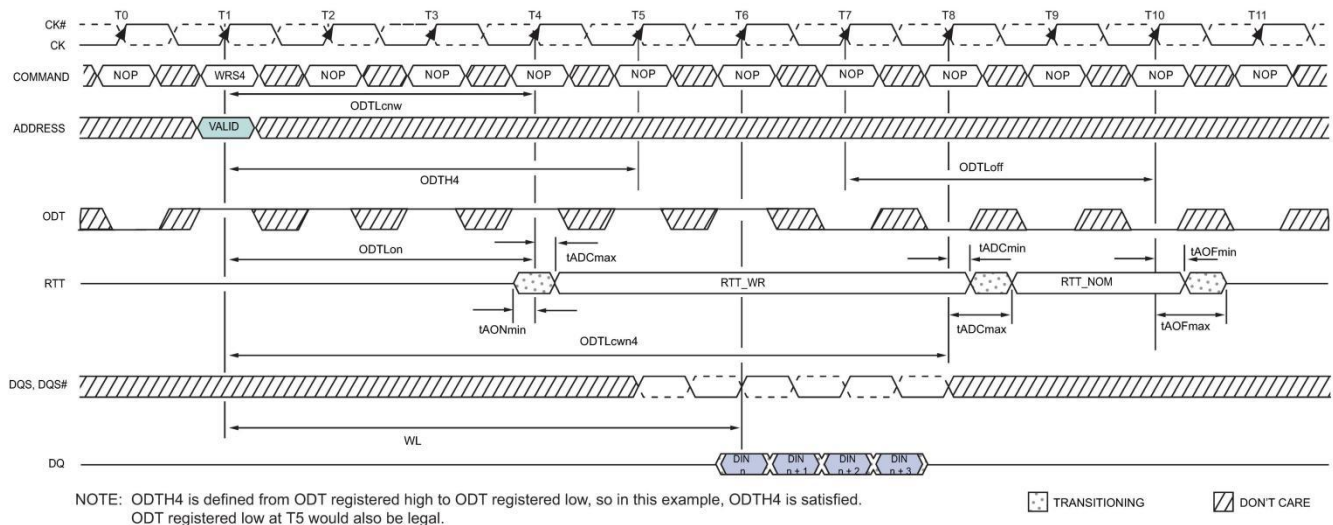


Figure 54 Dynamic ODT (ODT Pin Asserted with Write Command) Timing Diagram II

Dynamic ODT: ODT pin asserted together with a write command for a duration of 4 clock cycles

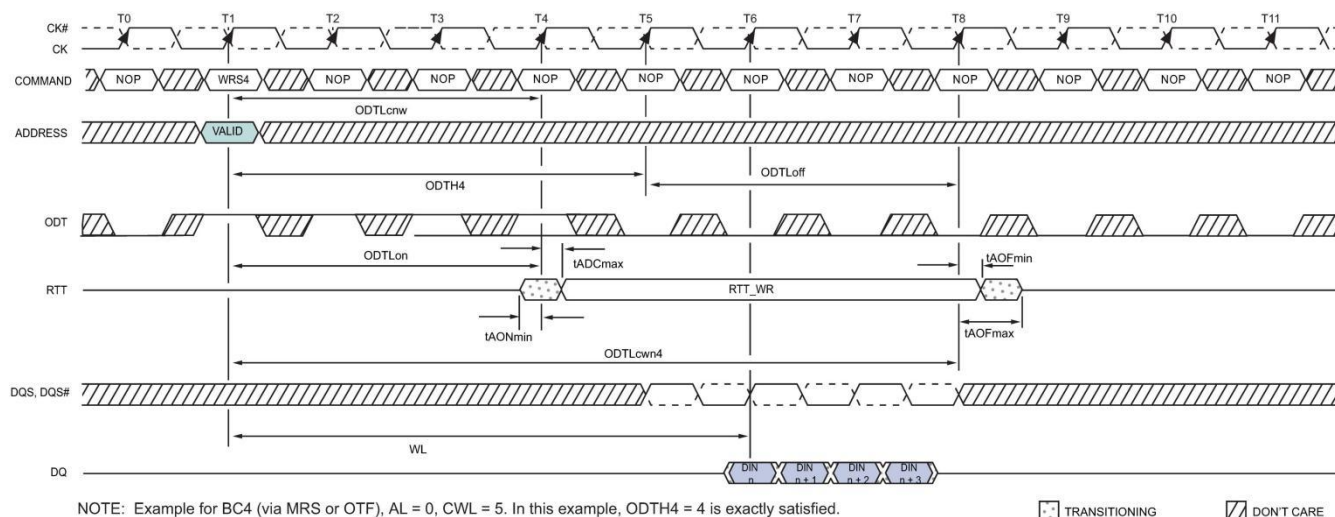


Figure 55 Dynamic ODT (ODT Pin Asserted with Write Command) Timing Diagram III

5.2.10.7 Asynchronous ODT Mode

When the DRAM is operating in DLL on mode, asynchronous ODT mode is selected, but the DLL is temporarily disabled (i.e., frozen) during precharge power-down (via Mode Register MR0 A12). According to the power-down mode definition, if the DLL is disabled during precharge power-down via Mode Register MR0 A12, the current state is precharge power-down mode.

In asynchronous ODT timing mode, the internal ODT command does not add additional latency (AL) relative to the external ODT command. In asynchronous ODT mode, the following timing parameters apply: tAONPD min/max, tAOFPD min/max.

Minimum RTT turn-on time ($t_{AONPD(min)}$) is the point when the on-die termination circuit leaves the high-impedance state and the ODT resistor begins to turn on. Maximum RTT turn-on time ($t_{AONPD(max)}$) is the moment when the ODT resistor is fully turned on.

RTT turn-on time ($t_{AONPD \text{ max}}$) is the moment when the ODT resistor is fully turned on.

tAONPDmin and tAONPDmax are measured from ODT being sampled high.

Minimum RTT turn-off time (tAOFPD min) is the point when the on-die termination circuit begins to turn off the ODT resistor. Maximum ODT turn-off time (tAOFPD max) is the moment when the ODT resistor is fully turned off.

(tAOFPDmax) is the point when the on-die termination reaches high impedance. tAOFPDmin and tAOFPDmax are measured from ODT being pulled low.

Asynchronous ODT Timing for DDR3 SDRAM with Fast ODT Transition: Ignore AL

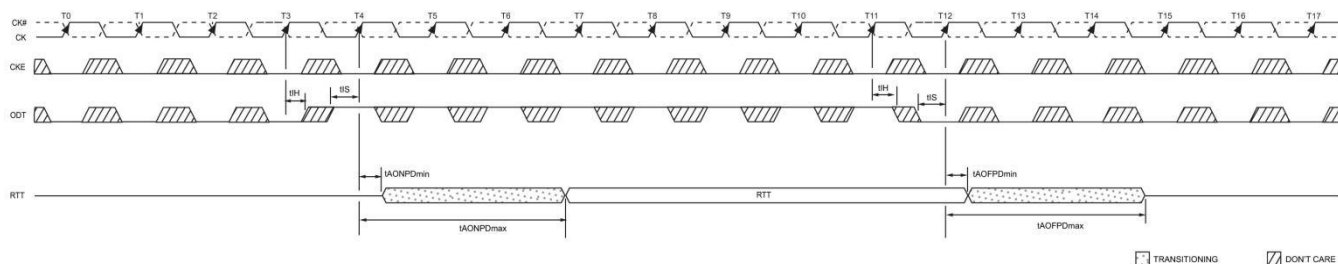


Figure 56 Asynchronous ODT Mode Timing Diagram

During precharge power-down, the ODT receiver remains active; however, since individual ADD/CMD receivers may be disabled,

no commands can be issued.

Read or write command.

Asynchronous ODT Timing Parameters

Table 46 Asynchronous ODT Timing Parameters

Abbreviation	Description	Min	Max	Unit
tAONPD	Asynchronous RTT turn-on delay (power-down with DLL frozen)	2	8.5	ns
tAOFPD	Asynchronous RTT turn-off delay (power-down with DLL frozen)	2	8.5	ns

Asynchronous ODT timing parameters for power-down with DLL frozen mode entry/exit cycles

Table 37 Key Parameters of ODT Turn-On/Turn-Off Timing

Description	Min	Max
ODT to RTT Turn-On Delay Time	$\min\{\text{ODTLon} \cdot \text{tCK} + \text{tAONmin}; \text{tAONPDmin}\}$ $\min\{(\text{WL}-2) \cdot \text{tCK} + \text{tAONmin}; \text{tAONPDmin}\}$	$\max\{\text{ODTLon} \cdot \text{tCK} + \text{tAONmax}; \text{tAONPDmax}\}$ $\max\{(\text{WL}-2) \cdot \text{tCK} + \text{tAONmin}, \text{tAONPDmax}\}$
ODT to RTT Turn-Off Delay Time	$\min\{\text{ODTloff} \cdot \text{tCK} + \text{tAOFmin}; \text{tAOFPDmin}\}$ $\min\{(\text{WL}-2) \cdot \text{tCK} + \text{tAOFmin}; \text{tAOFPDmin}\}$	$\max\{\text{ODTloff} \cdot \text{tCK} + \text{tAOFmax}; \text{tAOFPDmax}\}$ $\max\{(\text{WL}-2) \cdot \text{tCK} + \text{tAOFmax}; \text{tAOFPDmax}\}$
tANPD	WL-1	

Transition from Synchronous to Asynchronous ODT Mode during Power-Down Entry

If the DLL is selected to be frozen in precharge power-down mode by setting mode register MR0 A12 to '0', there will be a transition period before and after power-down entry, during which the DDR3 SDRAM may exhibit either synchronous or asynchronous ODT behavior.

The transition period is defined by parameters tANPD and tCPDED (min). tANPD equals (WL-1) and is counted backward in time from the clock cycle where CKE is first registered LOW. tCPDED (min) starts from the clock cycle where CKE is first registered LOW. The transition period begins at the start point of tANPD and ends at the end point of tCPDED (min). If a Refresh command is in progress when CKE goes LOW, the transition period ends at the later of tRFC (min) after the Refresh command and the end of tCPDED (min). Note that the actual start of tANPD is not included in the transition period, while the actual ends of tCPDED (min) and tRFC (min) are included in the transition period.

ODT assertion during the transition period may cause RTT changes as early as the smaller of tAONPDmin and (ODTLon*tCK+tAONmin), and as late as the larger of tAONPDmax and (ODTLon*tCK+tAONmax). ODT de-assertion during the transition period may occur as early as the smaller of tAOFPDmin and (ODTloff*tCK+tAOFmin) and as late as the larger of tAOFPDmax and (ODTloff*tCK+tAOFmax).

The larger of (ODTloff*tCK + tAOFmax) causes RTT change. Note that if the AL value is large, the range of RTT uncertainty becomes quite large. The figure below shows three different cases: ODT_A indicates synchronous behavior before tANPD; ODT_B indicates state change during the transition period; ODT_C indicates state change after the transition period.

Synchronous-to-Asynchronous Transition (DLL Frozen) Entry During Precharge Power-Down (AL=0; CWL=5; tANPD=WL-1=4)

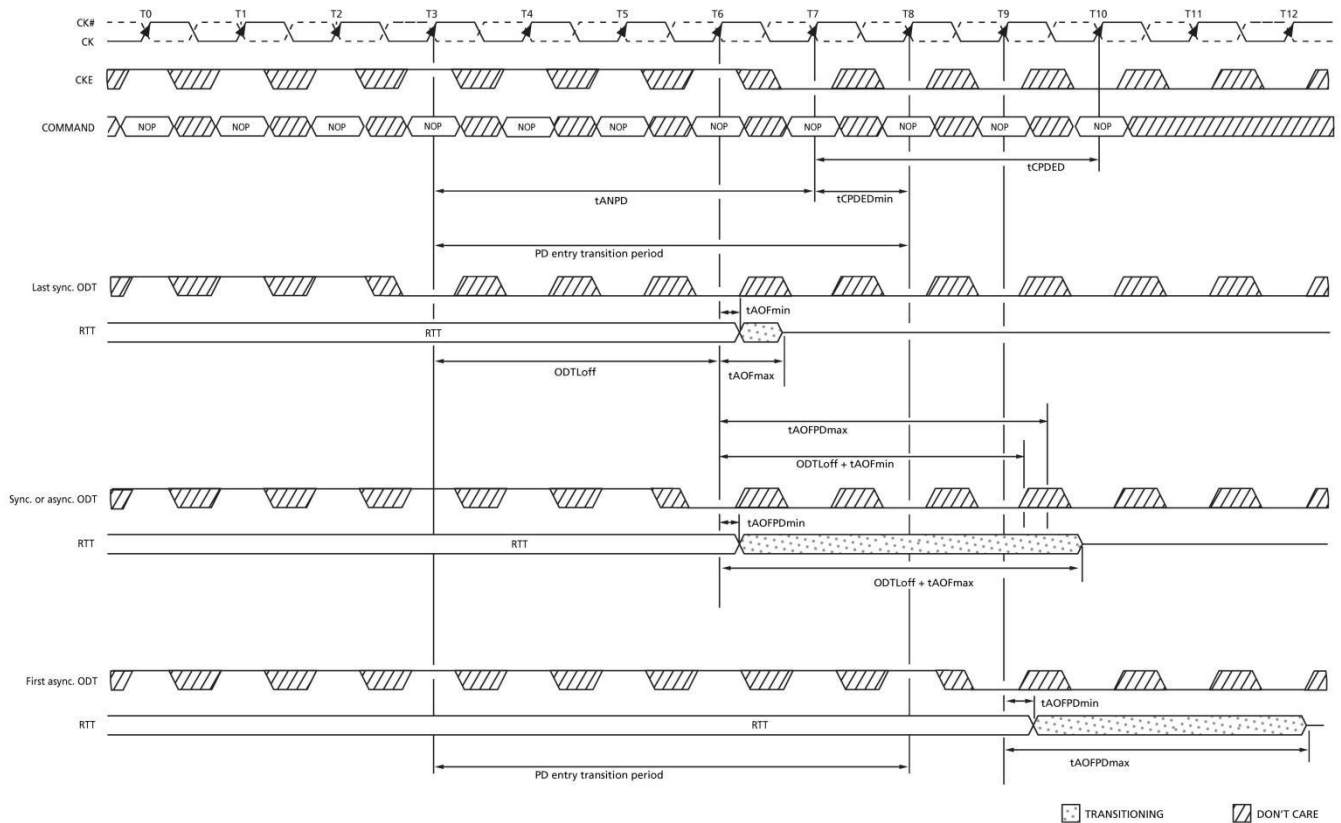


Figure 57 Precharge Power-Down Synchronous-to-Asynchronous Transition Timing Diagram

Synchronous-to-Asynchronous ODT Mode Transition During Power-Down Exit

If the DLL is selected to freeze in precharge power-down mode by setting the A12 bit of mode register MR0 to '0', there will also be a transition period before and after power-down exit during which the DDR3 SDRAM must be expected to respond synchronously or asynchronously to changes in ODT.

This transition period begins after t_{ANPD} from the first rising edge of CKE registered high, and ends after t_{XPDL} from the first rising edge of CKE registered high. t_{ANPD} equals (WL-1) and is counted (backwards) from the clock cycle where CKE is first sampled high.

ODT assertion during the transition period may cause RTT change as early as the smaller of $t_{AONPDmin}$ and $(ODTLon * t_{CK} + t_{AONmin})$, and as late as the larger of $t_{AONPDmax}$ and $(ODTLon * t_{CK} + t_{AONmax})$. ODT de-assertion during the transition period can be as early as the smaller of $t_{AOFDPmin}$ and $(ODTLoff * t_{CK} + t_{AOFmin})$ and as late as the larger of $t_{AOFDPmax}$ and $(ODTLoff * t_{CK} + t_{AOFmax})$ causes RTT change. Note that if the AL value is large, the range of RTT uncertainty becomes quite large. The figure below shows three different cases: ODT_C indicates asynchronous response before t_{ANPD} ; ODT_B indicates ODT state change during the transition period; ODT_A indicates ODT state change after the transition period with synchronous response.

Asynchronous to synchronous transition during precharge power-down (DLL frozen) exit (CL=6; AL=CL-1; CWL=5; t_{ANPD} =WL-1=9)

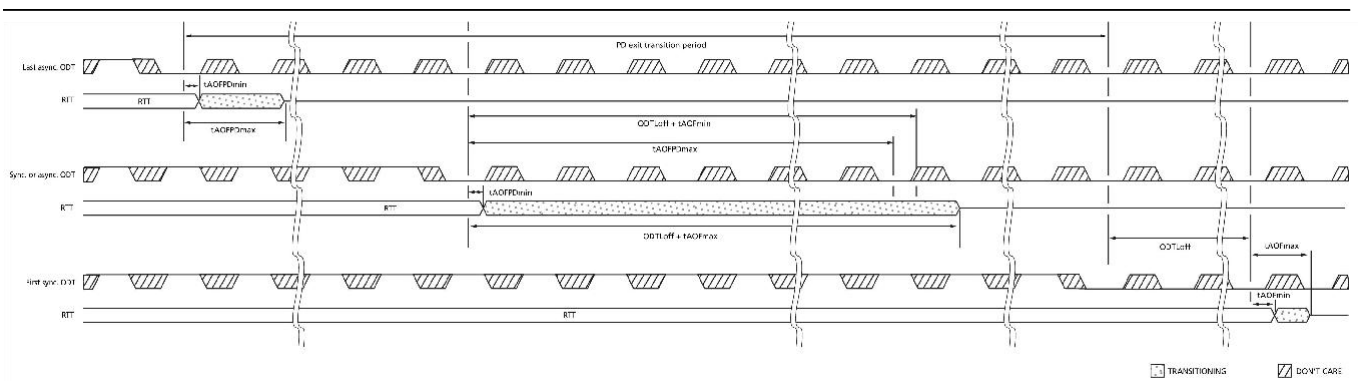


Figure 58 Timing diagram of asynchronous to synchronous transition during precharge power-down exit

5.2.10.8 Asynchronous to synchronous ODT mode during short CKE high and short CKE low periods

If the total time in precharge power-down state or idle state is very short, the transition periods for PD entry and PD exit may overlap. In this case, the response of the DDR3 SDRAM RTT to changes in the ODT state at the input can be synchronous or asynchronous from the state during the PD entry transition period to the end of the PD exit transition period (even if entry ends later than exit).

If the total time in idle state is very short, the transition periods for PD exit and PD entry may overlap. In this case, the response of the DDR3 SDRAM RTT to changes in the ODT state at the input can be synchronous or asynchronous from the state during the PD exit transition period to the end of the PD entry transition period. Note that in the figure below, it is assumed that no refresh command is in progress when entering idle state.

Transition period for short CKE cycle with overlapping entry and exit cycles (AL=0; WL=5; tANPD=WL-1=4)

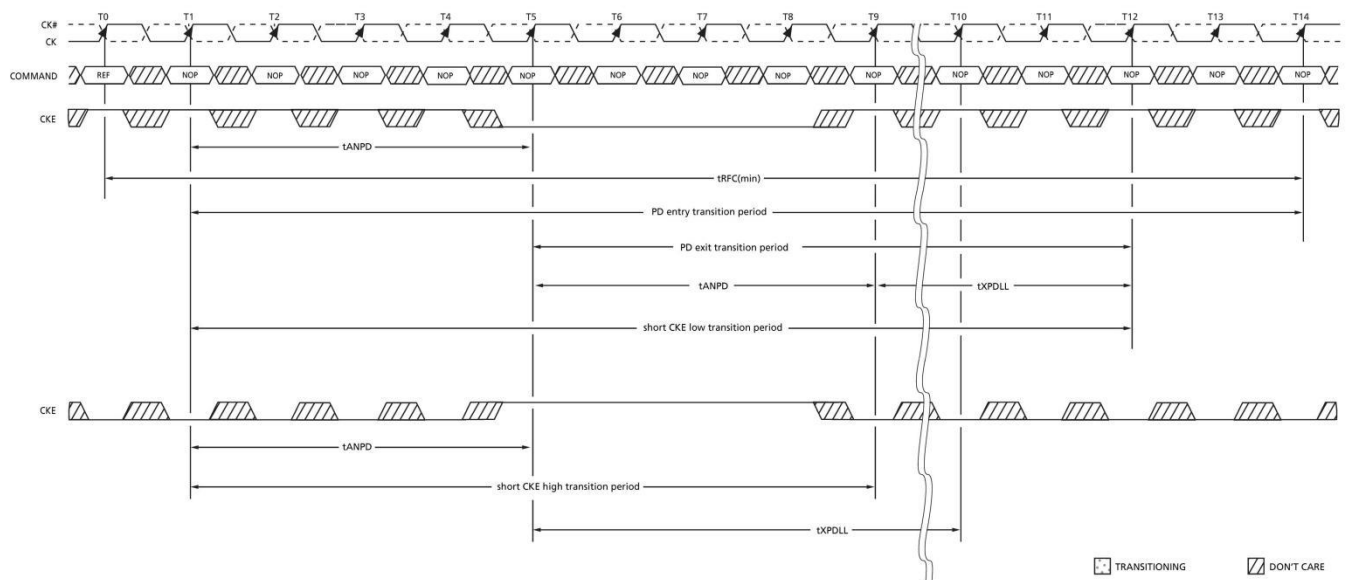


Figure 59 Timing diagram of overlapping entry/exit cycles

5.2.11 ZQ Calibration Command

5.2.11.1 ZQ Calibration Description

The ZQ calibration command is used to calibrate the DRAM Ron and ODT values. DDR3 SDRAM requires a longer time during initialization to calibrate the output driver and on-die termination matching circuits, and a relatively shorter time to perform

periodic calibration.

The ZQCL command is used to perform initial calibration during the power-up initialization sequence. This command can be issued by the controller at any time based on the system environment. The ZQCL command triggers the calibration engine inside the DRAM. Once calibration is complete, the calibration values are transferred from the calibration engine to the DRAM I/O, and the output driver and on-die termination matching values are updated.

The first ZQCL command issued after reset requires tZQinit clock cycles to perform full calibration and transfer values. All other ZQCL commands, except the first ZQCL command issued after RESET#, require tZQoper clock cycles.

The ZQCS command is used to perform periodic calibration to compensate for voltage and temperature variations. This command provides a shorter timing window for performing calibration and value transfer defined by the timing parameter tZQCS. During tZQinit, tZQoper, or tZQCS clock cycles, the controller should not perform any other activity on the DRAM channel. The quiet time on the DRAM channel allows calibration of the output driver and on-die termination matching values. Once DRAM calibration is complete, the DRAM should disable the ZQ current consumption path to reduce power.

Before the controller issues a ZQCL or ZQCS command, all banks must be precharged and the tRP timing must be satisfied.

After self-refresh exit, if no explicit ZQ calibration command is issued,

the DDR3 SDRAM will not perform I/O calibration. The earliest possible time for a ZQ calibration command (short or long) after self-refresh exit is tXS.

In a system where ZQ resistors are shared between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS timing between ranks.

ZQ Calibration Command Timing

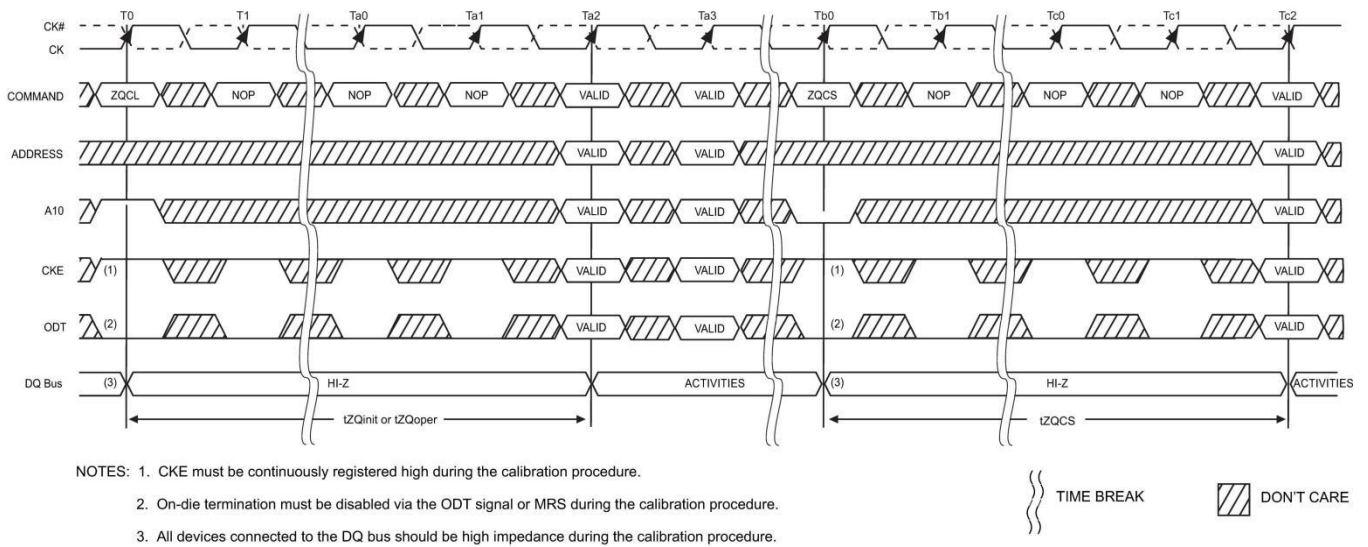


Figure 60 ZQ Calibration Command Timing Diagram

ZQ External Resistor, Tolerance, and Capacitive Load

To use the ZQ calibration function, a $240\ \Omega \pm 1\%$ external resistor is connected between the ZQ pin and ground. Each SDRAM may use an independent resistor, or if the ZQ calibration timing of each SDRAM does not overlap, one resistor can be shared between two SDRAMs. The total capacitive load on the ZQ pin must be limited.

5.2.11.2

DC Ratings

Table 48 DC Rating Parameters

Abbreviation	Parameter	Range	Unit	Notes
VDD	Voltage on VDD pin relative to VSS Voltage	-0.4~1.8	V	1,3
VDDQ	Voltage on VDDQ pin relative to VSS Voltage	-0.4~1.8	V	1,3
VIN/VOUT	Voltage on input/output pins relative to VSS Voltage	-0.4~1.8	V	1
TSTG	Storage Temperature	-55~100	°C	1,2

Note:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage temperature is the case surface temperature at the center/top of the DRAM.
- VDD and VDDQ must be within 300mV of each other at all times; when VDD and VDDQ are both less than 500mV, Vref must be no greater than 0.6×VDDQ; Vref may be equal to or less than 300mV.

Refresh parameters based on chip density

Table 49 Chip Density Refresh Cycle Time

Parameter	Abbreviation	1Gb	2Gb	4Gb	8Gb	Unit
REF command to ACT or REF command time	tRFC	110	160	260	350	ns

Temperature range

Table 50 Operating Temperature Range Information

Abbreviation	Parameter	Range TOPER	Unit	Notes
Commercial (C)	Operating Temperature Range	0~85	°C	1
	Extended Temperature Range	85~95	°C	1,2
Industrial (I)	Normal Operating Temperature Range	-40~85	°C	1
	Extended Temperature Range	85~95	°C	1,2

Note:

- Operating temperature TOPER is the case surface temperature at the center/top side of the DRAM.
- Some applications require the DRAM to operate in the extended temperature range between 85°C and 105 ° C case temperature. Full functionality is guaranteed within this range.

Specifications, subject to the following additional terms:

- Therefore, the refresh command frequency must be doubled, reducing the refresh interval t_{REFI} to 3.9 μs .
- If self-refresh operation is required in the extended temperature range, the extended temperature range self-refresh mode (Mode Register MR2 A6 = 0 and A7 = 1) with extended temperature range capability must be used, or the optional automatic self-refresh mode must be enabled.

5.2.12 AC and DC Operating Conditions

5.2.12.1 Recommended DC Operating Conditions

Table 51 Supply Voltage Operating Information

Abbreviation	Parameter		Range			Unit	Notes
			Min	Typ	Max		
VDD	Supply Voltage	DDR3	1.425	1.5	1.575	V	1,2
		DDR3	1.282	1.35	1.45	V	3,4,5,6
VDDQ	Output Supply Voltage	DDR3	1.425	1.5	1.575	V	1,2
		DDR3	1.282	1.35	1.45	V	3,4,5,6

Note:

- Under all conditions, VDDQ must be less than or equal to VDD.
- The VDDQ voltage rail is the same as VDD. AC parameters are measured when VDD and VDDQ are connected.
- The maximum DC value may not exceed 1.425 V. The DC value is the linear average of VDD/VDDQ over a long time period (e.g., 1 second).
- Input levels must not exceed this maximum limit and must conform to the DDR3 specification.
- At these supply voltages, the device operates according to the DDR3 specification.
- Once initialization for DDR3 operation is complete, DDR3 operation can only be used when VDD and VDDQ are switched to DDR3 operating voltages and the device is in reset state.
- VDD = VDDQ = 1.35V (1.283–1.45V), backward compatible with VDD = VDDQ = 1.5V $\pm$ 0.075V, supporting DDR3 devices backward compatible with 1.5V.

Applications.

5.2.12.2 Input DC and AC Measurement Levels

DDR3 AC and DC Logic Input Levels for Command and Address

Table 52 DC and AC Measurement Level Information I

Abbreviation	Parameter	DDR3-1066/1333/1600		DDR3-1866/2133		Unit	Notes
		Min	Max	Min	Max		
VIH.CA(DC100)	DC Input High Level	Vref+0.100	VDD	Vref+0.100	VDD	V	1,5
VIL.CA(DC100)	DC Input Low Level	VSS	Vref-0.100	VSS	Vref-0.100	V	1,6
VIH.CA(AC175)	AC Input High Level	Vref+0.175	Note 2			V	1,2,7
VIL.CA(AC175)	AC Input Low Level	Note 2	Vref-0.175			V	1,2,8
VIH.CA(AC150)	AC Input High	Vref+0.150	Note 2			V	1,2,7
VIL.CA(AC150)	AC Input Low	Note 2	Vref-0.150			V	1,2,8

VIH.CA(AC135)	AC Input High			Vref+0.135	Note 2	V	1,2,7
VIL.CA(AC135)	AC Input Low			Note 2	Vref-0.135	V	1,2,8
VIH.CA(AC125)	AC Input High			Vref+0.125	Note 2	V	1,2,7
VIL.CA(AC125)	AC Input Low			Note 2	Vref-0.125	V	1,2,8
VREFCA(DC)	ADD/CMD pins reference voltage	0.49*VDD	0.51*VDD	0.49*VDD	0.51*VDD	V	3,4,9

Note:

Note 1 For input pins other than RESET#, Vref = VrefCA(DC). Note 2

Please refer to the Overshoot and Undershoot Specifications.

Note 3 The AC peak noise on Vref may not allow Vref to deviate from VrefCA(DC) by more than +/-1% of VDD

(reference: about +/-15 mV). Note 4 Reference: about VDD/2 +/-15 mV.

Note 5: VIH(dc) is used as a simplified symbol for

VIH.CA(DC100). Note 6: VIL(dc) is used as a simplified symbol

for VIL.CA(DC100).

Note 7 VIH(ac) is used as an abbreviated symbol for VIH.CA(AC175), VIH.CA(AC150), VIH.CA(AC135) and

VIH.CA(AC125); when referenced to Vref+0.175V, use VIH.CA(AC175) value. When referenced to Vref+0.150V, use VIH.CA

(AC150) value. When referenced to Vref+0.135V, use VIH.CA(AC135) value. When referenced to Vref+0.125V, use

VIH.CA(AC125) value.

NOTE 8 VIL(ac) is used as a shorthand for VIL. VIL.CA(AC175), VIL.CA(AC150), VIL.CA(AC135) and VIL.CA(AC125). When

referenced to Vref-0.175V, use VIL.CA(AC175) value. When referenced to Vref-0.150V, use VIL.CA(AC150). When referenced to

Vref-0.135V, use VIL.CA(AC135) value. When referenced to Vref-0.125V, use VIL.CA(AC125) value.

NOTE 9 VrefCA(DC) is measured relative to VDD at the same point in time on the same device.

DDR3 AC and DC Logic Input Levels for Command and Address

Table 53 DC, AC Measurement Level Information II

Abbreviation	Parameter	DDR3-1066/1333/1600/1866/2133		Unit	Notes
		Min	Max		
VIH.CA(DC90)	DC input high voltage	Vref+0.09	VDD	V	1
VIL.CA(DC90)	DC input low voltage	VSS	Vref-0.09	V	1
VIH.CA(AC160)	AC Input High	Vref+0.16	Note 2	V	1,2
VIL.CA(AC160)	AC Input Low	Note 2	Vref-0.16	V	1,2
VIH.CA(AC135)	AC Input High	Vref+0.135	Note 2	V	1,2
VIL.CA(AC135)	AC Input Low	Note 2	Vref-0.135	V	1,2
VIH.CA(AC125)	AC Input High			V	1,2
VIL.CA(AC125)	AC Input Low			V	1,2

VREFCA(DC)	ADD/CMD pin reference voltage	0.49*VDD	0.51*VDD	V	3,4
-------------------	--------------------------------------	-----------------	-----------------	----------	------------

Note:

Note 1. Except for RESET, applies only to input pins. Vref = VrefCA

(DC). Note 2. See "Overshoot and Undershoot Specifications"

Note 3. AC peak noise on Vref may not allow Vref to deviate from Vref(DC) by more than

±0.1% VDD. Note 4. Reference: approximately VDD/2 ± 15 mV. For DDR3, VDD/2 ± 13.5 mV.

DDR3 AC and DC Logic Input Levels for DQ and DM

Table 54 DC and AC Measurement Level Information III

Abbreviation	Parameter	DDR3-1066/1333/1600		DDR3-1866/2133		Unit	Notes
		Min	Max	Min	Max		
VIH.CA(DC100) 00)	DC input high voltage	Vref+0.100	VDD	Vref+0.100	VDD	V	1,5
VIL.CA(DC100) 0)	DC input low voltage	VSS	Vref-0.100	VSS	Vref-0.100	V	1,6
VIH.CA(AC175) 75)	AC Input High	Vref+0.175	Note 2			V	1,2,7
VIL.CA(AC175) 5)	AC Input Low	Note 2	Vref-0.175			V	1,2,8
VIH.CA(AC150) 50)	AC Input High	Vref+0.150	Note 2			V	1,2,7
VIL.CA(AC150) 0)	AC Input Low	Note 2	Vref-0.150			V	1,2,8
VIH.CA(AC135) 35)	AC Input High			Vref+0.135	Note 2	V	1,2,7
VIL.CA(AC135) 5)	AC Input Low			Note 2	Vref-0.135	V	1,2,8
VREFCA(DC)	ADD/CMD pin reference voltage Pin reference voltage	0.49*VDD	0.51*VDD	0.49*VDD	0.51*VDD D	V	3,4,9

Note:

Note 1: For input-only pins except RESET, Vref = VrefCA(DC). Note 2:

Refer to the overshoot and undershoot specifications.

Note 3: The AC peak noise on Vref may not allow Vref to deviate from VrefCA(DC) by more than ±1% VDD (reference: approximately ±15 mV). Note 4: Reference: approximately VDD/2 ± 15 mV.

Note 5: VIH(dc) is used as a simplified symbol for

VIH.CA(DC100). Note 6: VIL(dc) is used as a simplified symbol

for VIL.CA(DC100).

Note 7: VIH(AC) is used as a simplified symbol for VIH_CA(AC175), VIH_CA(AC150), and VIH_CA(AC135).

When referencing $V_{ref} + 0.175\text{ V}$, use the $V_{IH.CA(AC175)}$ value. When referencing $V_{ref} + 0.150\text{ V}$, use the $V_{IH.CA(AC150)}$ value. When referencing $V_{ref} + 0.135\text{ V}$, use the $V_{IH.CA(AC135)}$ value.

Note 8: $V_{IL(AC)}$ is used as a shorthand for V_{IL} . $V_{IL.CA(AC175)}$, $V_{IL.CA(AC150)}$, $V_{IL.CA(AC135)}$. When V_{ref} is $V_{ref} - 0.175\text{ V}$, use the $V_{IL.CA(AC175)}$ value. When V_{ref} is $V_{ref} - 0.150\text{ V}$, use $V_{IL.CA(AC150)}$. When V_{ref} is $V_{ref} - 0.135\text{ V}$, use the $V_{IL.CA(AC135)}$ value.

Note 9: $V_{refCA(DC)}$ is measured with respect to V_{DD} at the same point in time on the same device.

DDR3 AC and DC logic input levels for DQ and DM

Table 55: DC and AC Measurement Level Information IV

Abbreviation	Parameter	DDR3-1066/1333/1600/1866/2133		Unit	Notes
		Min	Max		
$V_{IH.CA(DC90)}$	DC input high voltage	$V_{ref}+0.09$	V_{DD}	V	1
$V_{IL.CA(DC90)}$	DC input low voltage	V_{SS}	$V_{ref}-0.09$	V	1
$V_{IH.CA(AC160)}$	AC Input High	$V_{ref}+0.16$	Note 2	V	1,2
$V_{IL.CA(AC160)}$	AC Input Low	Note 2	$V_{ref}-0.16$	V	1,2
$V_{IH.CA(AC135)}$	AC Input High	$V_{ref}+0.135$	Note 2	V	1,2
$V_{IL.CA(AC135)}$	AC Input Low	Note 2	$V_{ref}-0.135$	V	1,2
$V_{IH.CA(AC125)}$	AC Input High			V	1,2
$V_{IL.CA(AC125)}$	AC Input Low			V	1,2
$V_{REFCA(DC)}$	ADD CMD Pin Reference Voltage	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	V	3,4

Note:

Note 1. Except for RESET, for input pins only. $V_{ref} = V_{refCA(DC)}$.

Note 2. See overshoot and undershoot specifications.

Note 3. AC peak noise on V_{ref} may not allow V_{ref} to deviate from $V_{ref(DC)}$ by more than $\pm 0.1\% V_{DD}$. Note 4. Reference: approximately $V_{DD}/2 \pm 15\text{ mV}$. For DDR3, $V_{DD}/2 \pm 13.5\text{ mV}$.

5.2.12.2.1 V_{ref} Tolerance

The DC and AC tolerance limits for the reference voltages V_{refCA} and V_{refDQ} are shown in the figure below. It shows the effective reference voltage as a function of time.

Reference voltage $V_{ref}(t)$. (V_{ref} represents both V_{refCA} and V_{refDQ} .)

$V_{ref}(DC)$ is the linear average of $V_{ref}(t)$ over a very long period of time (e.g., 1 second). This average must meet the minimum and maximum requirements on the previous page. Additionally, $V_{ref}(t)$ may temporarily deviate from $V_{ref}(DC)$ by no more than $\pm 1\%$ of V_{DD} .

The voltage levels for $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$, and $V_{IL}(DC)$ used in setup and hold time measurements are dependent on V_{ref} . Should be understood as $V_{ref}(DC)$.

This clarifies that the DC variation of V_{ref} affects the absolute voltage the signal must reach to achieve a valid high or low level, thereby affecting the measured setup and hold times. System timing and voltage budgets must consider the deviation of $V_{ref}(DC)$ from the optimal position within the data eye of the input signal.

This also clarifies that the DRAM setup/hold specification and derating need to include the timing and voltage associated with V_{ref} AC noise. Since the

timing and voltage effects caused by AC noise on V_{ref} up to the specified limit (1% of V_{DD}) are included in the DRAM timing and its associated derating.

Schematic Diagram of $V_{ref}(DC)$ Tolerance and V_{ref} AC Noise Limits

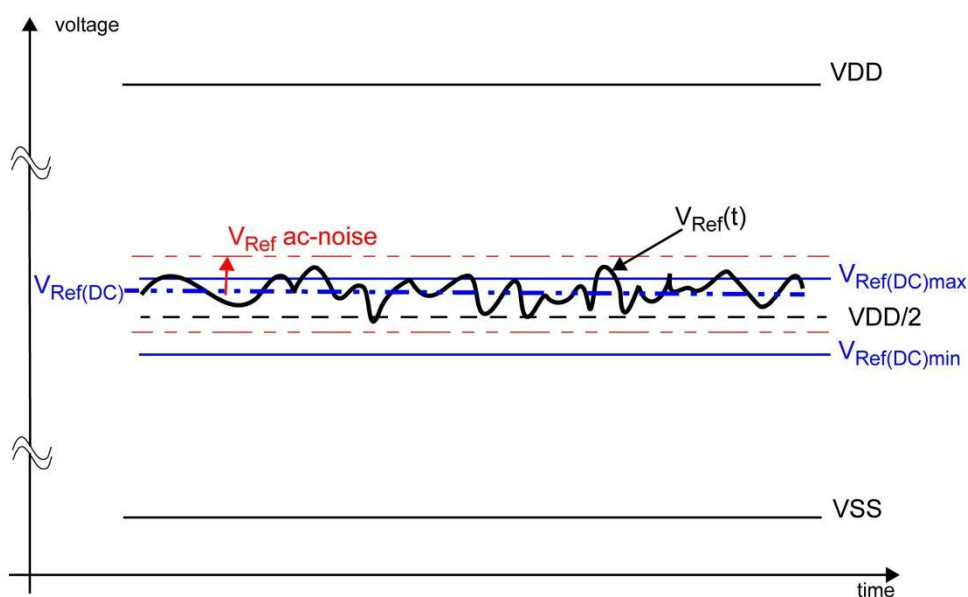


Figure 61 $V_{ref}(DC)$ Tolerance and AC Noise Limits Schematic Diagram

DDR3 Differential AC and DC Input Levels for Clock (CK-CK#) and Strobe (DQS-DQS#)

Table 56 AC and DC Input Voltage Information for DQS-DQS#

Abbreviation	Parameter	DDR3-1066/1333/1600/1866/2133		Unit	Notes
		Min	Max		
VIHdiff	Differential Input High Level	+0.200	Note 3	V	1
VILdiff	Differential Input Low Level	Note 3	-0.200	V	1
VIHdiff(ac)	Differential Input High Level (AC)	$2 \times (V_{IH}(ac) - V_{ref})$	Note 3	V	2
VILdiff(ac)	Differential Input Low Level (AC)	Note 3	$2 \times (-V_{IH}(ac) + V_{ref})$	V	2
DDR3-1066/1333/1600					

VIHdiff	Differential Input High	+0.180	Note 3	V	1
VILdiff	Differential Input Low	Note 3	-0.180	V	1

$V_{IHdiff(ac)}$	Differential Input High (AC)	$2 \times (V_{IH(ac)} - V_{ref})$	Note 3	V	2
$V_{ILdiff(ac)}$	Differential Input Low (AC)	Note 3	$2 \times (-V_{IH(ac)} + V_{ref})$	V	2

Note:

Note 1. Used to define differential signal slew rate.

Note 2. For CK-CK#, use V_{IH}/V_{IL} (AC) of ADD/CMD and VREFCA; for DQS-DQS#, DQSL, DQSL#, DQSU, DQSU#, use V_{IH}/V_{IL} (AC) of DQ and VREFDQ. If reduced AC high or low levels are used for a signal group, the reduced levels also apply to that signal group.

Note 3. These values are not defined; however, the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# are defined such that the corresponding limits for single-ended signals ($V_{IH}(DC)$ max, $V_{IL}(DC)$ min) are controlled within the overshoot and undershoot limits.

Definition of Differential AC Swing and "Time above AC Level"

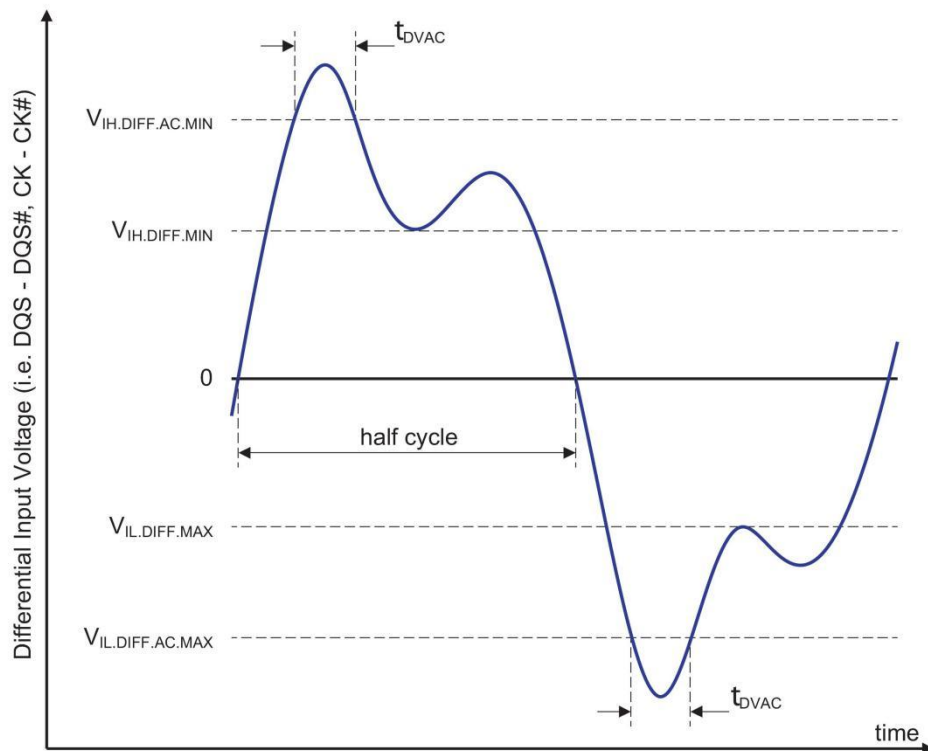


Figure 62 Differential AC Swing and Overshoot Time Definition

DDR3 CK-CK# and DQS-DQS# Ringback Allowable Time (t_{DVAC})

Table 57 DQS-DQS# Ringback Allowable Time (t_{DVAC})

Slew Rate (V/ns)	DDR3-1066/1333/1600						DDR3-1866/2133			
	t_{DVAC} (ps) @ $V_{IH(ac)}/V_{IL(ac)}$ differential =350mV		t_{DVAC} [ps] @ $ V_{IH}/L_{diff}(ac) $ =300mV		t_{DVAC} [ps] @ $ V_{IH}/L_{diff}(ac) $ = DQS - DQS# only		t_{DVAC} [ps] @ $ V_{IH}/L_{diff}(ac) $ =300mV		t_{DVAC} [ps] @ $ V_{IH}/L_{diff}(ac) $ = CK - CK# only	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max

>4.0	189		201		163		168		176	
4.0	189		201		163		168		176	
3.0	162		179		140		147		154	
2.0	109		134		95		105		111	
1.8	91		119		80		91		97	
1.6	69		100		62		74		78	
1.4	40		76		37		52		56	
1.2	Note		44		5		22		24	
1.0	Note		Note		Note		Note		Note	
<1.0	Note		Note		Note		Note		Note	

Note:

The rising input differential signal must be equal to or greater than the $V_{IHdiff}(AC)$ level, and the falling input differential signal must be equal to or less than the $V_{ILdiff}(AC)$ level.

Level.

Single-Ended Requirements for Differential Signals

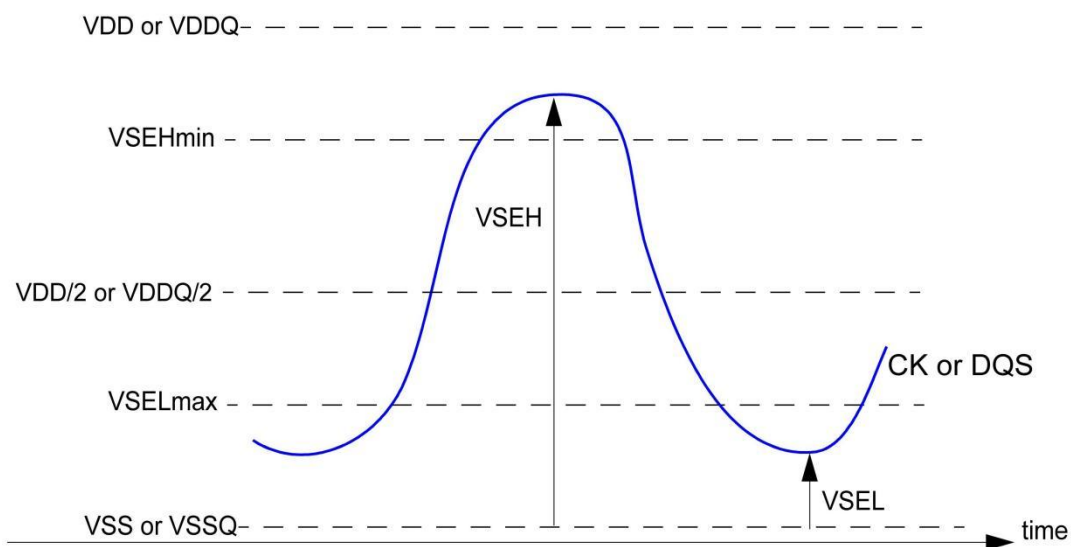


Figure 63 Single-Ended Requirements for Differential Signals

Each individual component of the differential signals (CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, or DQSU#) must also meet certain requirements for single-ended signals.

CK and CK# must approximately reach V_{SEHmin}/V_{SELmax} in each half cycle (approximately equal to the ac levels of the ADD/CMD signals (V_{IH}

(ac)/ $V_{IL}(ac)$)).

Note that the applicable ac levels for ADD/CMD and DQ may differ due to pin speed, etc. For example, if $V_{IH150}(ac)/V_{IL150}(ac)$ is used for ADD/CMD signals, these ac levels also apply to the single-ended signals CK# and CK.

Single-Ended Levels for CK, DQS, DQSL, DQSU, CK#, DQS#, or DQSU#

Table 58 Single-Ended Level Information for Differential Signals

Abbreviation	Parameter	DDR3-1066/1333/1600/1866/2133		Unit	Notes
		Min	Max		
VSEH	Single-Ended High Level for Strobe	$(VDDQ/2)+0.175$	Note 3	V	1,2
	Single-Ended High Level for CK, CK#	$(VDDQ/2)+0.175$	Note 3	V	1,2
VSEL	Single-Ended Low Level for Strobe	Note 3	$(VDDQ/2)-0.175$	V	1,2
	Single-Ended Low Level for CK, CK#	Note 3	$(VDDQ/2)-0.175$	V	1,2

Note:

1. For CK and CK#, use VIH(ac)/VIL(ac) of ADD/CMD; for strobes (DQS, DQSL, DQSU, DQS#, DQSL#, DQSU#), use VIH(ac)/VIL(ac) of DQ.
2. VIH(ac)/VIL(ac) for DQ are based on VREFDQ; VIH(ac)/VIL(ac) for ADD/CMD are based on VREFCA. If reduced ac-high or ac-low levels are used for a signal group, the reduced levels also apply to that signal group.
3. These values are not defined, but the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# must be within the corresponding limits for single-ended signals (VIH(dc) max, VIL(dc) min) and meet overshoot and undershoot limits.

Differential Input Crosspoint Voltage

To ensure tight setup and hold times and output skew parameters relative to clock and strobe, each crosspoint voltage of the differential input signals (CK, CK# and DQS, DQS#) must meet the requirements in the table below. The differential input crosspoint voltage V_{ix} is measured from the actual crossing point of the true and complemented signals to the midpoint between VDD and VSS.

Figure 64 Differential Input Crosspoint Voltage Diagram Crosspoint Voltage of Differential Input Signals (CK, DQS)

Table 59 Differential Input Signal Crosspoint Voltage Information (CK, DQS)

Abbreviation	Parameter		Min	Max	Unit	Notes
VIX(CK)	Differential input cross of CK, CK# relative to VDD/2 point voltage	DDR3	-150	150	mV	1
			-175	175	mV	1
		DDR3	-150	150	mV	2

VIX(DQS)	DQS, DQS#	DDR3	-150	150	mV	1
	Differential input cross point voltage relative to VDD/2	DDR3	-150	150	mV	1

Note:

4. The relationship between VIX Min/Max and VSEL/VSEH shall satisfy the following requirements

$$(VDD/2) + VIX(min) - VSEL > 25 \text{ mV};$$

$$VSEH - ((VDD/2) + VIX(max)) \geq 25 \text{ mV};$$

5. The extended range of VIX is only allowed for clock signals, and only if the single-ended clock input signals CK and CK# are monotonic, the single-ended swings VSEL and VSEH are at least $VDD/2 \pm 250 \text{ mV}$, and the differential slew rate of CK-CK# is greater than 3 V/ns .

Differential input signal slew rate

The definition and measurement of the input slew rate for differential signals (CK, CK# and DQS, DQS#) are as follows.

Table 60 Differential Input Slew Rate Definition and Measurement

Description	Measurement		Definition
	From	TO	
Slew rate for differential input rising edge (CK-CK#, DQS-DQS#)	VILdiffmax	VIHdiffmin	$[VIHdiffmin - VILdiffmax] / \Delta TR$
Slew rate for differential input falling edge (CK-CK#, DQS-DQS#)	VIHdiffmin	VILdiffmax	$[VIHdiffmin - VILdiffmax] / \Delta TR$

The differential signals (i.e., CK-CK# and DQS-DQS#) must be linear between these thresholds.

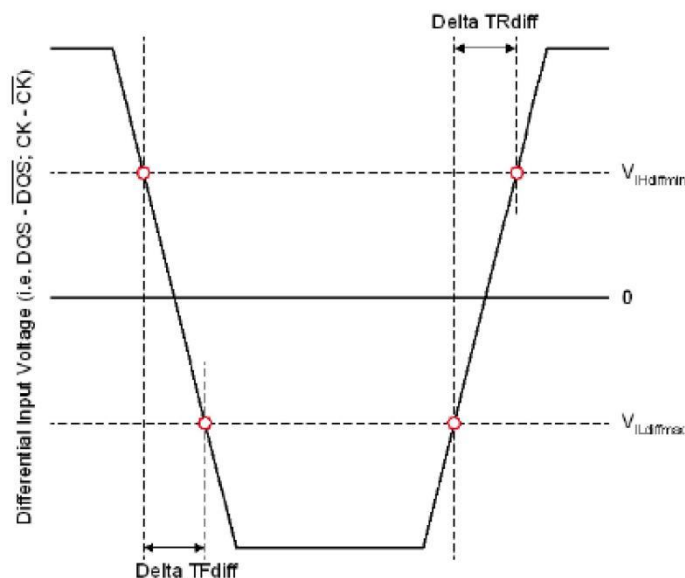


Figure 65 Differential Signal Measurement Diagram

Input Slew Rate Definition for Single-Ended Signals

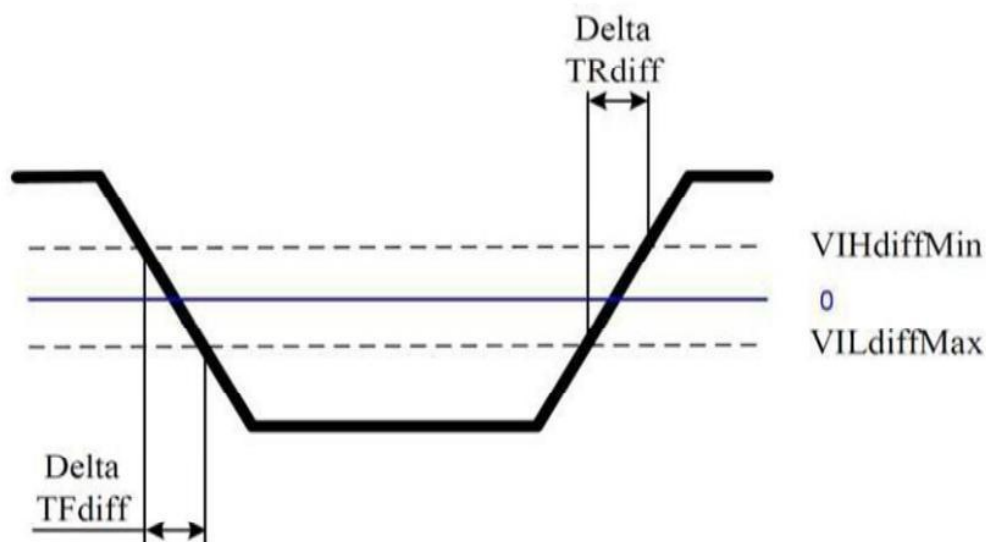


Figure 66 Input Slew Rate Definition for Single-Ended Signals

5.2.12.2.2 Output AC and DC Measurement Levels

Single-Ended AC and DC Output Levels

Table 61 Single-Ended AC and DC Output Voltages

Abbreviation	Parameter	Value	Unit	Notes
VOH(DC)	DC output high measurement level (IV curve linear)	$0.8 \times VDDQ$	V	
VOM(DC)	DC output middle measurement level (IV curve linear)	$0.5 \times VDDQ$	V	
VOL(DC)	DC output low measurement level (from IV curve linear)	$0.2 \times VDDQ$	V	
VOH(AC)	AC output high measurement level (for output SR)	$V_{TT} + 0.1 \times VDDQ$	V	1
VOL(AC)	AC output low measurement level (for output SR)	$V_{TT} - 0.1 \times VDDQ$	V	1

Note: $\pm 0.1 VDDQ$ swing based on approximately 50% of static single-ended output high or low swing, driver impedance 40Ω , effective test load 25Ω to $V_{TT} = VDDQ/2$.

Differential AC and DC output levels.

Abbreviation	Parameter	Value	Unit	Notes
	AC Differential Output High Measurement Level (for output SR)			
	AC Differential Output Low Measurement Level (for output SR)			

Note: The $\pm 0.2 VDDQ$ swing is approximately 50% of the static differential output high swing or low swing, with driver

impedance of 40Ω , and the effective test load for each differential output is 25Ω to $V_{TT} = VDDQ/2$.

Single-ended output slew rate

Table 63 Single-ended Output Slew Rate

Description	Measurement		Definition
	From	To	

Rising edge single-ended output slew rate	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta t_{rise}$
Falling edge single-ended output slew rate	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta t_{fall}$
Output slew rate is guaranteed by design and characterization and may not be production tested.			

Single-Ended Output Slew Rate Definition

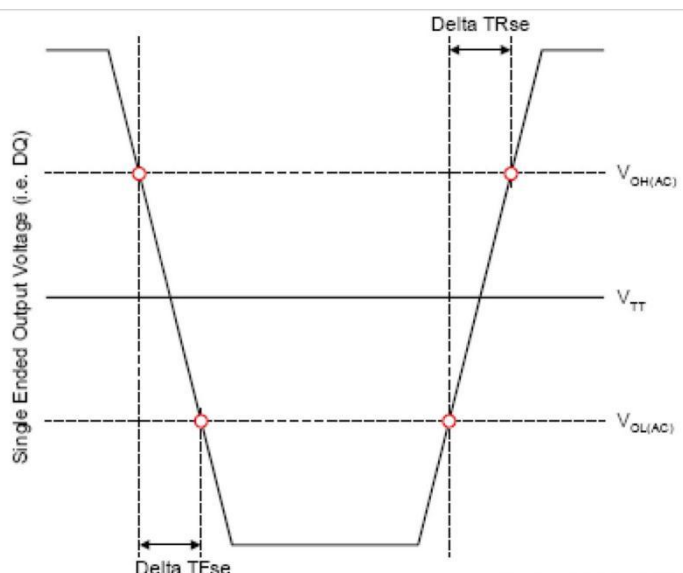


Figure 67 Single-Ended Output Slew Rate Definition Diagram

Single-Ended Output Slew Rate Parameters

Table 64 Single-Ended Output Slew Rate Parameters

Parameter	Abbreviation	Grade	Min	Max	Unit
Single-Ended Output Slew Rate	SRQse	DDR3	2.5	5	V/ns
		DDR3	1.75	5	V/ns

Note:

SR: Slew Rate.

Q: Output data (similar to DQ, representing data output). se: Single-ended signal.

For Ron = RZQ/7 setting.

Note 1): In both cases, the maximum slew rate of 6 V/ns applies to a single DQ signal within a byte lane.

Case 1 is defined as a single DQ signal within a byte lane that is switching in a particular direction (from high to low or from low to high), while all remaining DQ signals in the same byte lane are static (i.e., they remain high or low).

Case 2 is defined for a single DQ signal within a byte lane that is switching in one direction (from high to low or from low to high), while all remaining DQ signals in the same byte lane switch in the opposite direction (i.e., from low to high or from high to low, respectively). For the remaining DQ signals switching in the opposite direction, the maximum limit of 5 V/ns applies.

Differential Output Slew Rate

Table 65 Differential Output Slew Rate

Description	Measurement		Definition
	From	To	
Rising Edge Differential Output Slew Rate	$V_{OLDiff(AC)}$	$V_{OHDiff(AC)}$	$[V_{OHDiff(AC)} - V_{OLDiff(AC)}] / \Delta t_{rise}$

Falling Edge Differential Output Slew Rate	VOHdiff (AC)	VOLDiff (AC)	$[VOHdiff(AC) - VOLDiff(AC)] / \Delta t_{Rse}$
Output slew rate is guaranteed by design and characterization and may not be production tested.			

Differential Output Slew Rate Definition

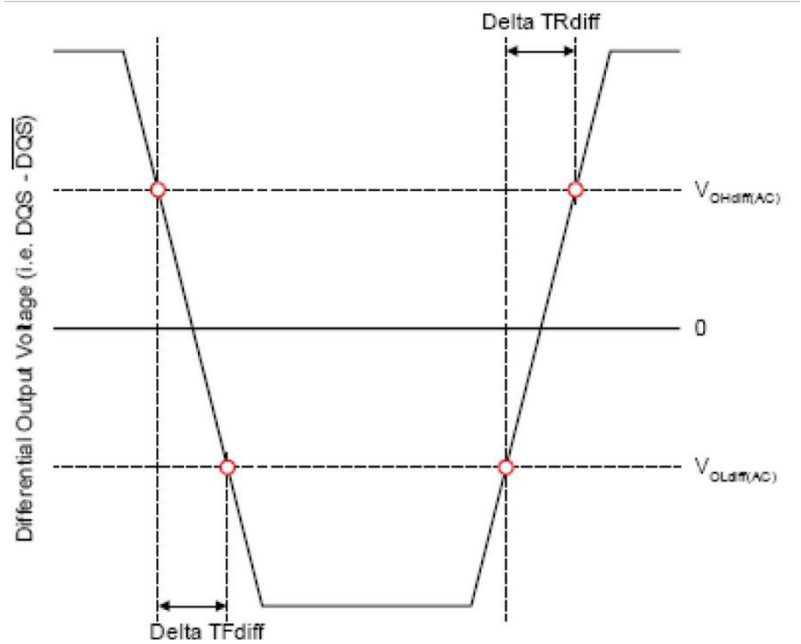


Figure 68 Differential Output Slew Rate Definition

Differential Output Slew Rate Parameters

Table 66 Differential Output Slew Rate Parameters

Parameter	Abbreviation	Grade	1066/1333/1600		1866/2133		Unit
			Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	DDR3	5	10	5	12	V/ns
		DDR3	3.5	12	3.5	12	V/ns

Note:

SR: Slew rate.

Q: data output (e.g., DQ read data); diff: differential signal. For Ron = RZQ/7 setting.

Reference Load for AC Timing and Output Slew Rate

The figure below shows the effective reference load of 25 ohms used to define the device's AC timing parameters and output slew rate measurements.

It does not represent any specific system environment nor describe the actual load used in production testing. System designers should use IBIS or other simulation tools to map the timing reference load to the system environment. Manufacturer test conditions typically consist of one or more coaxial transmission lines with test termination.

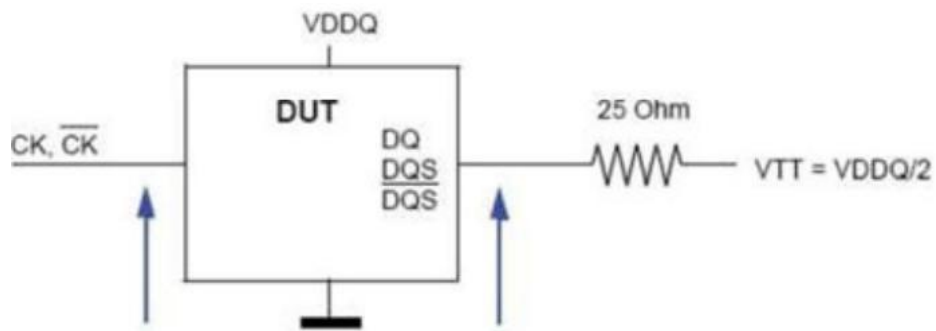


Figure 69 AC Timing and Output Slew Rate Circuit Diagram

Overshoot and Undershoot Characteristics

AC Overshoot and Undershoot Characteristics for Address and Control Pins

Table 67 Address and Control Pin AC Overshoot and Undershoot Characteristics Information

Parameter	1066	1333	1600	1866	2133	Unit
Maximum Peak Amplitude Allowed in Overshoot Region	0.4	0.4	0.4	0.4	0.4	V
Maximum Peak Amplitude Allowed in Overshoot Region	0.4	0.4	0.4	0.4	0.4	V
Maximum Peak Amplitude Allowed in Undershoot Region	0.4	0.4	0.4	0.4	0.4	V
Maximum Peak Amplitude Allowed in Undershoot Region	0.4	0.4	0.4	0.4	0.4	V
Maximum overshoot area below VDD	0.5	0.4	0.33	0.28	0.25	V-ns
Maximum Undershoot Area Below VSS	0.5	0.4	0.33	0.28	0.25	V-ns
(A0 – A14, BA0 – BA3, CS#, RAS#, CAS#, WE#, CKE, ODT)						

Note 1: The sum of the applied voltage (VDD) and the peak overshoot voltage must not exceed the absolute maximum DC rating.

Note 2: The sum of the applied voltage (VDD) and the peak undershoot voltage must not exceed the absolute maximum DC rating.

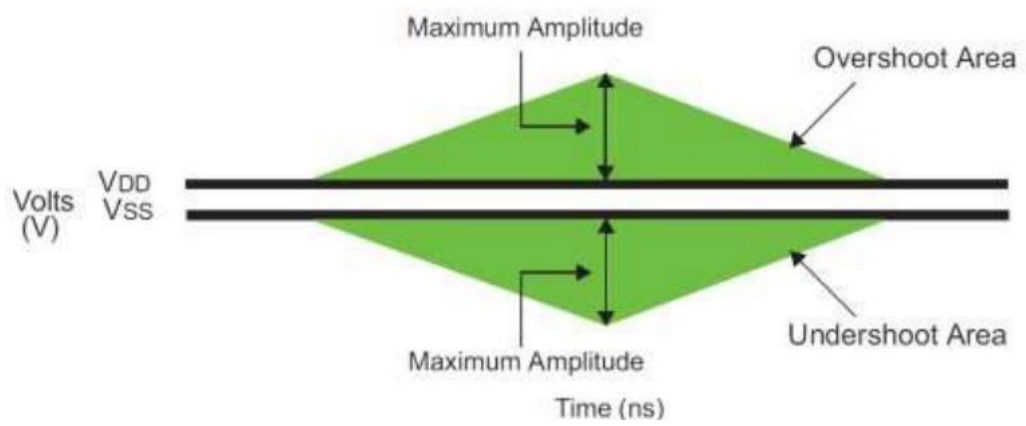


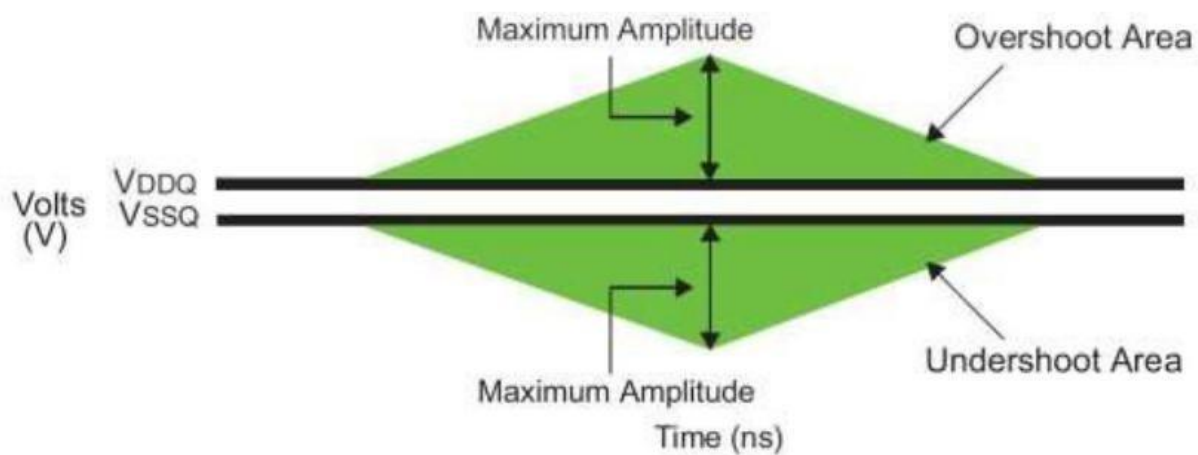
Figure 70 Overshoot and Undershoot Characteristics

Table 68 AC Overshoot and Undershoot Characteristics for Clock, Data, Strobe, and Mask

List	1066	1333	1600	1866	2133	Unit
Maximum Peak Amplitude Allowed in Overshoot Region	0.4	0.4	0.4	0.4	0.4	V
Maximum Peak Amplitude Allowed in Undershoot Region	0.4	0.4	0.4	0.4	0.4	V
Maximum Overshoot Area Above VDD	0.19	0.15	0.13	0.11	0.10	V-ns
Maximum Undershoot Area Below VSS	0.19	0.15	0.13	0.11	0.10	V-ns
(CK,CK#,DQ,DQS,DQS#,DM)						

Note 1: The sum of the applied voltage (VDD) and the peak overshoot voltage must not exceed the absolute maximum DC rating.

Note 2: The sum of the applied voltage (VDD) and the peak undershoot voltage must not exceed the absolute maximum DC rating.

*Figure 71 Overshoot and Undershoot Characteristics Circuit Diagram*

5.2.12.2.3 34 Ohm Output Driver DC Electrical Characteristics

The function of the output buffer is described as follows. The output driver impedance R_{ON} is defined by the value of the external reference resistor R_{ZQ} as follows:

$R_{ON34} = R_{ZQ}/7$ (nominal $34.4\ \Omega \pm 10\%$, nominal $R_{ZQ} = 240\ \Omega$). The

pull-up and pull-down resistors (R_{ONPu} and R_{ONPd}) are defined as follows:

$R_{ONPu} = (V_{DDQ} - V_{out}) / |I_{out}|$, with R_{ONPd} turned off (1)

$R_{ONPd} = V_{out} / |I_{out}|$, with R_{ONPu} turned off (2)

Output Driver: Voltage and Current Definitions

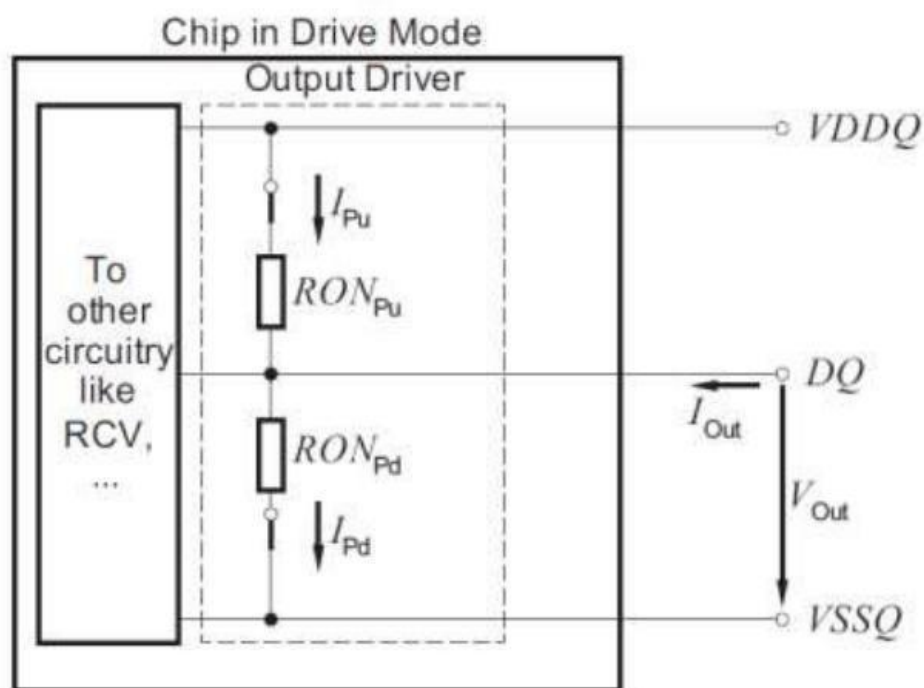


Figure 72 Output Driver Circuit Diagram

Output Driver DC Electrical Characteristics, assuming RZQ = 240 Ω ; full operating temperature range; after proper ZQ calibration

Table 69 Output Driver DC Electrical Characteristics I

RONom	Resistance	Vout	Min	Nom	Max	Organization	Notes
DDR3							
34 ohms	RON34Pd	VOLdc = $0.2 \times VDDQ$	0.6	1.0	1.1	RZQ/7	1,2,3
		VOMdc = $0.5 \times VDDQ$	0.9	1.0	1.1	RZQ/7	1,2,3
		VOHdc = $0.8 \times VDDQ$	0.9	1.0	1.4	RZQ/7	1,2,3
	RON34Pu	VOLdc = $0.2 \times VDDQ$	0.9	1.0	1.4	RZQ/7	1,2,3
		VOMdc = $0.5 \times VDDQ$	0.9	1.0	1.1	RZQ/7	1,2,3
		VOHdc = $0.8 \times VDDQ$	0.6	1.0	1.1	RZQ/7	1,2,3
40 ohms	RON40Pd	VOLdc = $0.2 \times VDDQ$	0.6	1.0	1.1	RZQ/6	1,2,3
		VOMdc = $0.5 \times VDDQ$	0.9	1.0	1.1	RZQ/6	1,2,3
		VOHdc = $0.8 \times VDDQ$	0.9	1.0	1.4	RZQ/6	1,2,3
	RON40Pu	VOLdc = $0.2 \times VDDQ$	0.9	1.0	1.4	RZQ/6	1,2,3

		$VOMdc = 0.5 \times VDDQ$	0.9	1.0	1.1	RZQ/6	1,2,3
		$VOHdc = 0.8 \times VDDQ$	0.6	1.0	1.1	RZQ/6	1,2,3
Mismatch between pull-up and pull-down Mismatch, MMPuPd		$VOMdc = 0.5 \times VDDQ$	-10		+10	%	1,2,4

Table 70 Output Driver DC Electrical Characteristics II

RONom	Resistance	Vout	Min	Nom	Max	Organization	Notes
DDR3							
34 ohms	RON34Pd	$VOLdc = 0.2 \times VDDQ$	0.6	1.0	1.15	RZQ/7	1,2,3
		$VOMdc = 0.5 \times VDDQ$	0.9	1.0	1.15	RZQ/7	1,2,3
		$VOHdc = 0.8 \times VDDQ$	0.9	1.0	1.45	RZQ/7	1,2,3
	RON34Pu	$VOLdc = 0.2 \times VDDQ$	0.9	1.0	1.45	RZQ/7	1,2,3
		$VOMdc = 0.5 \times VDDQ$	0.9	1.0	1.15	RZQ/7	1,2,3
		$VOHdc = 0.8 \times VDDQ$	0.6	1.0	1.15	RZQ/7	1,2,3
40 ohms	RON40Pd	$VOLdc = 0.2 \times VDDQ$	0.6	1.0	1.15	RZQ/6	1,2,3
		$VOMdc = 0.5 \times VDDQ$	0.9	1.0	1.15	RZQ/6	1,2,3
		$VOHdc = 0.8 \times VDDQ$	0.9	1.0	1.45	RZQ/6	1,2,3
	RON40Pu	$VOLdc = 0.2 \times VDDQ$	0.9	1.0	1.45	RZQ/6	1,2,3
		$VOMdc = 0.5 \times VDDQ$	0.9	1.0	1.15	RZQ/6	1,2,3
		$VOHdc = 0.8 \times VDDQ$	0.6	1.0	1.15	RZQ/6	1,2,3
Mismatch between pull-up and pull-down , MMPuPd		$VOMdc = 0.5 \times VDDQ$	-10		+10	%	1,2,4

Note:

1. After calibration under stable voltage and temperature conditions, tolerance limits are specified. For the behavior of tolerance limits when temperature or voltage changes after calibration, see the following sections on voltage and temperature sensitivity.
2. Tolerance limits are specified under conditions $VDDQ = VDD$ and $VSSQ = VSS$.
3. It is recommended to calibrate the pull-down and pull-up output driver impedance at $0.5VDDQ$. Other calibration schemes can be used to achieve the

linearity specification. For example, at 0.2VDDQ and 0.8VDDQ.✖

4. Pull-up to Pull-down Mismatch Measurement Definition, MMPuPd:

$$\text{Measure RONPu and RONPd, but at 0.5VDDQ: } \text{MMPuPd} = \frac{\text{RONPu} - \text{RONPd}}{\text{RONNom}} \times 100\%$$

Output Driver Temperature and Power Supply Sensitivity

If calibrated temperature and/or voltage, the tolerance limits will expand according to the table below. $\Delta T = T - T$ (at calibration); $\Delta V = VDDQ - VDDQ$ (at

calibration); $VDD = VDDQ$

Note: dRONdT and dRONdV are not production tested, but are verified by design and characterization.

Output Sensitivity Definition

Table 71 Output Sensitivity Definition

List	Min	Max	Unit
RONPu@VOHdc	0.6-dRONdTH*DeltaTI-dRONdVH*DeltaVI	1.1+dRONdTH*DeltaTI-dRONdVH*DeltaVI	RZQ/7
RONPu@VOMdc	0.9-dRONdTM*DeltaTI-dRONdVH*DeltaVI	1.1+dRONdTM*DeltaTI-dRONdVH*DeltaVI	RZQ/7
RONPu@VOLdc	0.6-dRONdTL*DeltaTI-dRONdVH*DeltaVI	1.1+dRONdTL*DeltaTI-dRONdVH*DeltaVI	RZQ/7

Output Driver Supply Voltage and Temperature Sensitivity

Table 72 Output Driver Supply Voltage and Temperature Sensitivity Information

Speed Bin	DDR3-1066/1333		DDR3-1600		Unit
List	Min	Max	Min	Max	
dRONdTM	0	1.5	0	1.5	%/°C
dRONdVM	0	0.15	0	0.13	%/V
dRONdTL	0	1.5	0	1.5	%/°C
dRONdVL	0	0.15	0	0.13	%/mV
dRONdTH	0	1.5	0	1.5	%/°C
dRONdVH	0	0.15	0	0.13	%/mV

Note:

These parameters may not be production tested. They are verified by design and characterization.

5.2.12.3 On-Die Termination (ODT) Levels and I-V Characteristics

The on-die termination resistance R_{TT} is defined by bits A9, A6, and A2 of Mode Register MR1. ODT applies to pins DQ, DM, DQS, DQS#

and TDQS, TDQS# (x8 mode only) pins.✖

The function of on-die termination is represented in the figure below. The

$$R_{TTPu} = \frac{VDDQ - V_{out}}{|I_{out}|}$$

individual pull-up and pull-down resistors (R_{TTPu} and R_{TTPd}) are defined

as follows: With R_{TTPd} turned off (3)

With R_{TTPu} turned off, the definition of voltage and current

for on-die termination (4)

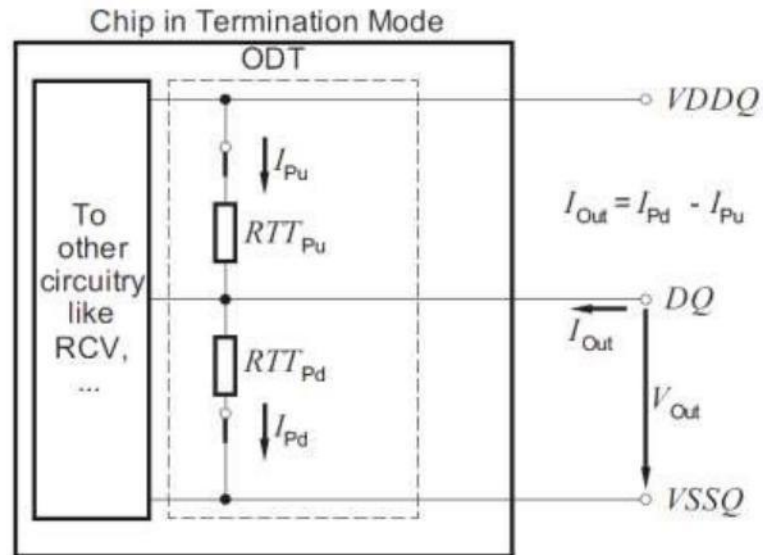


Figure 73 On-Die Termination (ODT) Circuit Diagram

5.2.12.3.1 ODT DC Electrical Characteristics

The following table summarizes the ODT DC electrical characteristics. The values of RTT60Pd120, RTT60Pu120, RTT120Pd240, RTT120Pu240, RTT40Pu80, RTT30Pd80, RTT30Pd60, RTT30Pu60, RTT20Pd40, RTT20Pu40 are not specification requirements but may be used as design guidelines:

ODT DC Electrical Characteristics, assuming $RZQ = 240 \Omega \pm 1\%$ over full operating temperature range; after proper ZQ calibration (DDR3).

Table 73 ODT DC Characteristic Information I

MR1 A9,A6,A2	RTT	Resistance	Vout	Min	Nom	Max	Unit	Notes
0,1,0	120ohm	RTT120Pd240	$VOL_{dc} = 0.2 \times VDDQ$	0.6	1.0	1.15	RZQ	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.15	RZQ	1,2,3,4
			$VOH_{dc} = 0.8 \times VDDQ$	0.9	1.0	1.45	RZQ	1,2,3,4
		RTT120Pu240	$VOL_{dc} = 0.2 \times VDDQ$	0.9	1.0	1.45	RZQ	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.15	RZQ	1,2,3,4
			$VOH_{dc} = 0.8 \times VDDQ$	0.6	1.0	1.15	RZQ	1,2,3,4
		RTT120	VIL(ac) TO VIH(ac)	0.9	1.0	1.65	RZQ/2	1,2,5
0,0,1	60ohm	RTT60Pd120	$VOL_{dc} = 0.2 \times VDDQ$	0.6	1.0	1.15	RZQ/2	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.15	RZQ/2	1,2,3,4
			$VOH_{dc} = 0.8 \times VDDQ$	0.9	1.0	1.45	RZQ/2	1,2,3,4

		RTT60Pu120	$VOL_{dc}=0.2 \times VDDQ$	0.9	1.0	1.45	RZQ/2	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.15	RZQ/2	1,2,3,4
			$VOH_{dc}=0.8 \times VDDQ$	0.6	1.0	1.15	RZQ/2	1,2,3,4
		RTT60	VIL(ac) TO VIH(ac)	0.9	1.0	1.65	RZQ/4	1,2,5
0,1,1	40ohm	RTT40Pd80	$VOL_{dc}=0.2 \times VDDQ$	0.6	1.0	1.15	RZQ/3	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.15	RZQ/3	1,2,3,4
			$VOH_{dc}=0.8 \times VDDQ$	0.9	1.0	1.45	RZQ/3	1,2,3,4
		RTT40Pu80	$VOL_{dc}=0.2 \times VDDQ$	0.9	1.0	1.45	RZQ/3	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.15	RZQ/3	1,2,3,4
			$VOH_{dc}=0.8 \times VDDQ$	0.6	1.0	1.15	RZQ/3	1,2,3,4
		RTT40	VIL(ac) TO VIH(ac)	0.9	1.0	1.65	RZQ/6	1,2,5
1,0,1	30ohm	RTT30Pd60	$VOL_{dc}=0.2 \times VDDQ$	0.6	1.0	1.15	RZQ/2	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.15	RZQ/2	1,2,3,4
			$VOH_{dc}=0.8 \times VDDQ$	0.9	1.0	1.45	RZQ/2	1,2,3,4
		RTT(30, PU60)	$VOL_{dc}=0.2 \times VDDQ$	0.9	1.0	1.45	RZQ/2	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.15	RZQ/2	1,2,3,4
			$VOH_{dc}=0.8 \times VDDQ$	0.6	1.0	1.15	RZQ/2	1,2,3,4
		RTT30	VIL(ac) TO VIH(ac)	0.9	1.0	1.65	RZQ/4	1,2,5
1,1,0	20ohm	RTT(20, PD40)	$VOL_{dc}=0.2 \times VDDQ$	0.6	1.0	1.15	RZQ/6	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.15	RZQ/6	1,2,3,4
			$VOH_{dc}=0.8 \times VDDQ$	0.9	1.0	1.45	RZQ/6	1,2,3,4
		RTT(20, PU40)	$VOL_{dc}=0.2 \times VDDQ$	0.9	1.0	1.45	RZQ/6	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.15	RZQ/6	1,2,3,4
			$VOH_{dc}=0.8 \times VDDQ$	0.6	1.0	1.15	RZQ/6	1,2,3,4

		RTT20	VIL(ac) TO VIH(ac)	0.9	1.0	1.65	RZQ/12	1,2,5
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Deviation of VM from VDDQ/2 and DVM	-5		+5	%	1,2,5,6
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ODT DC Electrical Characteristics, assuming RZQ = 240 Ω +/-1% over full operating temperature range; after proper ZQ calibration (DDR3).

Table 74 ODT DC Characteristic Information II

MR1 A9,A6,A2	RTT	Resistance	Vout	Min	Nom	Max	Unit	Notes
0,1,0	120ohm	RTT120Pd240	$VOL_{dc}=0.2 \times VDDQ$	0.6	1.0	1.1	RZQ	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.1	RZQ	1,2,3,4
			$VOH_{dc}=0.8 \times VDDQ$	0.9	1.0	1.4	RZQ	1,2,3,4
		RTT120Pu240	$VOL_{dc}=0.2 \times VDDQ$	0.9	1.0	1.4	RZQ	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.1	RZQ	1,2,3,4
			$VOH_{dc}=0.8 \times VDDQ$	0.6	1.0	1.1	RZQ	1,2,3,4
		RTT120	VIL(ac) TO VIH(ac)	0.9	1.0	1.6	RZQ/2	1,2,5
0,0,1	60ohm	RTT60Pd120	$VOL_{dc}=0.2 \times VDDQ$	0.6	1.0	1.1	RZQ/2	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.1	RZQ/2	1,2,3,4
			$VOH_{dc}=0.8 \times VDDQ$	0.9	1.0	1.4	RZQ/2	1,2,3,4
		RTT60Pu120	$VOL_{dc}=0.2 \times VDDQ$	0.9	1.0	1.4	RZQ/2	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.1	RZQ/2	1,2,3,4
			$VOH_{dc}=0.8 \times VDDQ$	0.6	1.0	1.1	RZQ/2	1,2,3,4
		RTT60	VIL(ac) TO VIH(ac)	0.9	1.0	1.6	RZQ/4	1,2,5
0,1,1	40ohm	RTT40Pd80	$VOL_{dc}=0.2 \times VDDQ$	0.6	1.0	1.1	RZQ/3	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.1	RZQ/3	1,2,3,4
			$VOH_{dc}=0.8 \times VDDQ$	0.9	1.0	1.4	RZQ/3	1,2,3,4
		RTT40Pu80	$VOL_{dc}=0.2 \times VDDQ$	0.9	1.0	1.4	RZQ/3	1,2,3,4
			$0.5 \times VDDQ$	0.9	1.0	1.1	RZQ/3	1,2,3,4
			$VOH_{dc}=0.8 \times VDDQ$	0.6	1.0	1.1	RZQ/3	1,2,3,4

		RTT40	VIL(ac) TO VIH(ac)	0.9	1.0	1.6	RZQ/6	1,2,5
1,0,1	30ohm	RTT30Pd60	VOLdc=0.2XVDDQ	0.6	1.0	1.1	RZQ/2	1,2,3,4
			0.5XVDDQ	0.9	1.0	1.1	RZQ/2	1,2,3,4
			VOHdc=0.8XVDDQ	0.9	1.0	1.4	RZQ/2	1,2,3,4
		RTT30Pu60	VOLdc=0.2XVDDQ	0.9	1.0	1.4	RZQ/2	1,2,3,4
			0.5XVDDQ	0.9	1.0	1.1	RZQ/2	1,2,3,4
			VOHdc=0.8XVDDQ	0.6	1.0	1.1	RZQ/2	1,2,3,4
		RTT30	VIL(ac) TO VIH(ac)	0.9	1.0	1.6	RZQ/4	1,2,5
1,1,0	20ohm	RTT20Pd40	VOLdc=0.2XVDDQ	0.6	1.0	1.1	RZQ/6	1,2,3,4
			0.5XVDDQ	0.9	1.0	1.1	RZQ/6	1,2,3,4
			VOHdc=0.8XVDDQ	0.9	1.0	1.4	RZQ/6	1,2,3,4
		RTT20Pu40	VOLdc=0.2XVDDQ	0.9	1.0	1.4	RZQ/6	1,2,3,4
			0.5XVDDQ	0.9	1.0	1.1	RZQ/6	1,2,3,4
			VOHdc=0.8XVDDQ	0.6	1.0	1.1	RZQ/6	1,2,3,4
		RTT20	VIL(ac) TO VIH(ac)	0.9	1.0	1.6	RZQ/12	1,2,5
Deviation of VM from VDDQ/2 and DVM				-5		+5	%	1,2,5,6

Note:

1. After calibration using stable voltage and temperature, tolerance limits are specified. For the behavior of tolerance limits if temperature or voltage changes after calibration, refer to the following section on voltage and temperature sensitivity.
2. Tolerance limits are specified under conditions $VDDQ = VDD$ and $VSSQ = VSS$.
3. It is recommended to calibrate pull-down and pull-up ODT resistors at $0.5VDDQ$. Other calibrations may be used to achieve the linearity specifications shown above.✕
4. Not a specification requirement, but a design guideline.
5. Measurement Definition of RTT:

Apply $V_{IH}(ac)$ to the pin under test and measure current I , calculate resistance $R = V_{IH}(ac) / I$; then apply $V_{IL}(ac)$ to the same pin and measure voltage V , calculate resistance $R = V / V_{IL}(ac)$.

$$RTT = \frac{VIH(ac) - VIL(ac)}{I(VIH(ac)) - I(VIL(ac))}$$

6. Measurement Definition of VM and DVM:

Under no-load condition, measure the voltage (VM) at the test pin (midpoint):

$$\Delta MV = \left(\frac{2 \times VM}{VDDQ} - 1 \right) \times 100$$

If the calibrated temperature and/or voltage change, the tolerance limits will expand according to the table below. $\Delta T = T - T_{cal}$, $\Delta V = VDDQ - VDDQ_{cal}$.

During calibration); VDD = VDDQ.

ODT Sensitivity Definition

Table 75 ODT Sensitivity Definition

List	Min	Max	Unit
RTT	$0.9 - dRTTdT * \Delta T - dRTTdV * \Delta V$	$1.6 + dRTTdT * \Delta T + dRTTdV * \Delta V$	RZQ/2,4,6,8,12
dRTTdT	0	1.5	%/°C
dRTTdV	0	0.15	%/mV

Note: These parameters may not require production testing. They are verified by design and characterization.

5.2.12.3.2 On-Die Termination (ODT) Test Load Timing

Unlike timing measurements, the ODT timing reference load is defined in the figure below.

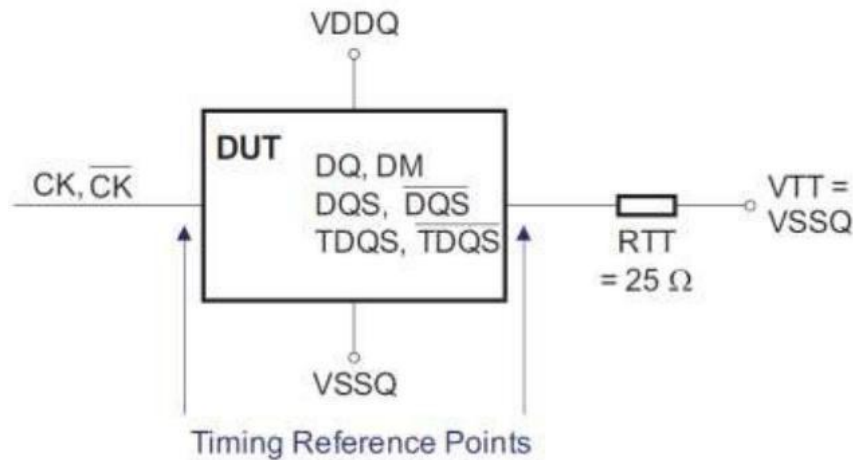


Figure 74 ODT Reference Load Circuit Diagram

5.2.12.3.3 On-Die Termination (ODT) Timing Definitions

The definitions of tAON, tAONPD, tAOF, tAOFPD, and tADC are provided in the following table and subsequent figures.

Table 76 ODT Timing Definitions

Abbreviation	Starting Point Definition	End Point Definition
tAON	rising edge of CK - CK#, defined by the ODTLon endpoint	extrapolated point at VSSQ
tAONPD	rising edge of CK - CK# with ODT first registered HIGH	extrapolated point at VSSQ
tAOF	rising edge of CK - CK#, defined by the ODTLoff endpoint	extrapolated point at VRTT_Nom
tAOFPD	rising edge of CK - CK# with ODT first registered LOW	extrapolated point at VRTT_Nom
tADC	Rising edge of CK-CK#, defined by ODTLcnw and ODTLcwn	End point: extrapolated points at VRTT and VRTT_Nom

		respectively
--	--	--------------

	End point definition for ODTLcwn 8	
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Reference settings for ODT timing measurements

Table 77 ODT Timing Measurement Reference Setting Information

Measurement parameters	RTT_Nom	RTT_Wr	DDR3		DDR3	
			VSW1[V]	VSW2[V]	VSW1[V]	VSW2[V]
tAON	RZQ/4	NA	0.05	0.10	0.05	0.10
	RZQ/12	NA	0.10	0.20	0.10	0.20
tAONPD	RZQ/4	NA	0.05	0.10	0.05	0.10
	RZQ/12	NA	0.10	0.20	0.10	0.20
tAOF	RZQ/4	NA	0.05	0.10	0.05	0.10
	RZQ/12	NA	0.10	0.20	0.10	0.20
tAOFPD	RZQ/4	NA	0.05	0.10	0.05	0.10
	RZQ/12	NA	0.10	0.20	0.10	0.20
tADC	RZQ/12	RZQ/12	0.20	0.30	0.20	0.25

Definition of tAON

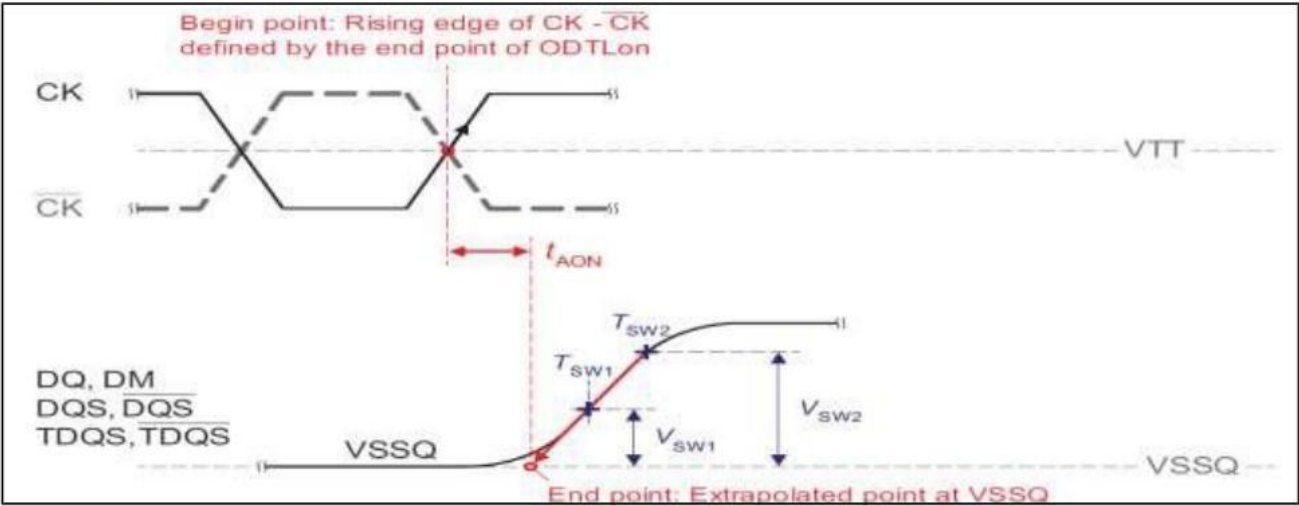


Figure 75 Signal Timing and Voltage Parameter Definition Diagram I

Definition of tAONPD

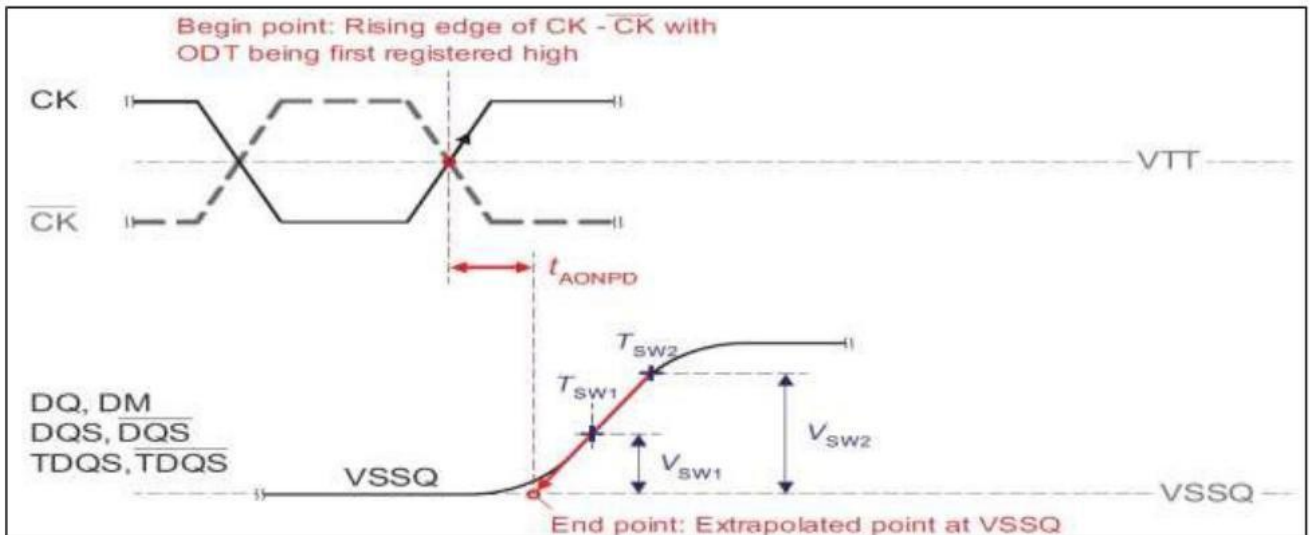


Figure 76 Signal Timing and Voltage Parameter Definition Diagram II

Definition of tAOF

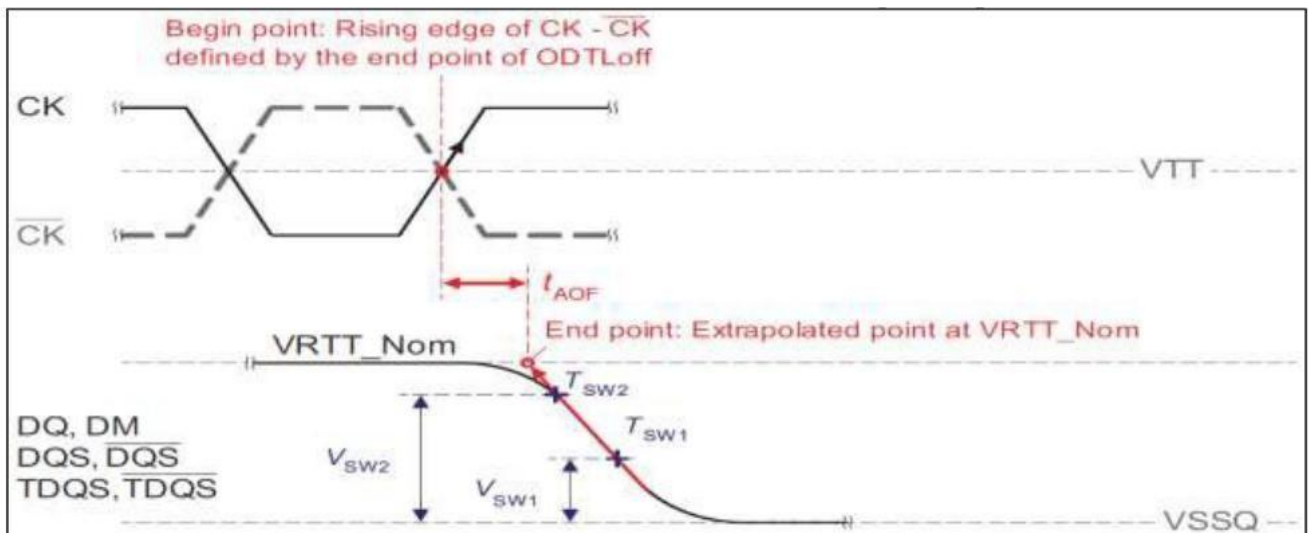


Figure 77 Signal Timing and Voltage Parameter Definition Diagram III

Definition of tAOFPD

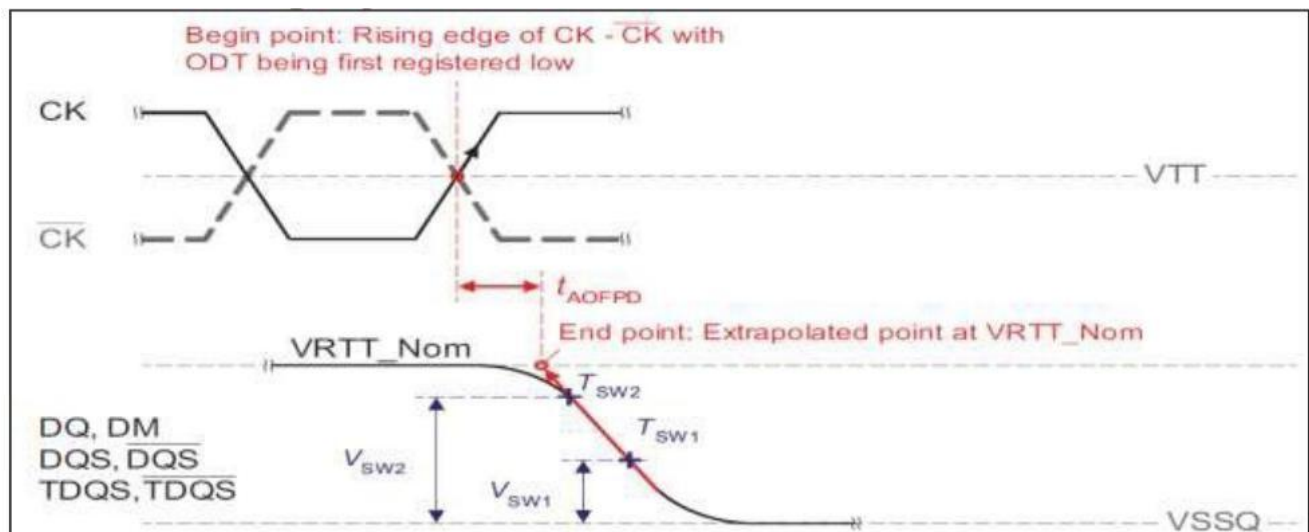


Figure 78 Signal Timing and Voltage Parameter Definition Diagram IV

Definition of tADC

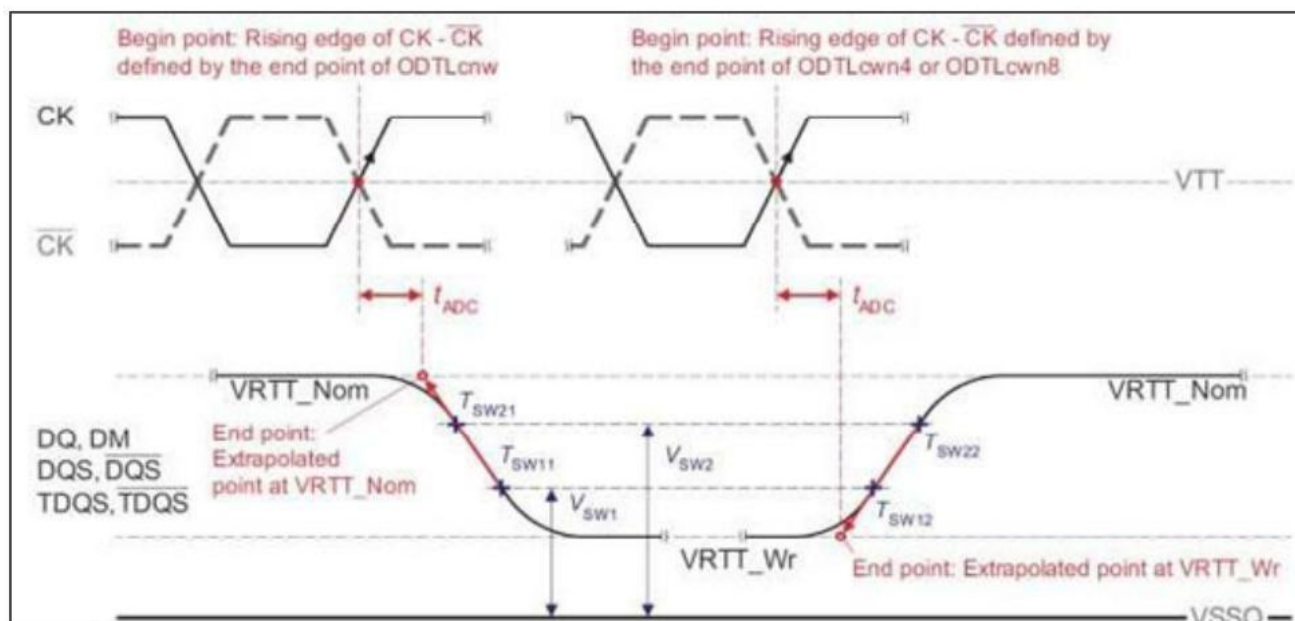


Figure 79 Timing and Voltage Parameter Definition Diagram V

Input/Output Capacitance

Table 78 Input/Output Capacitance Information

Abbreviation	Parameter	1066		1333		1600		1866		2133		Unit bit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CIO	Input/Output Capacitance (DQ, DM, DQS, DQS#, TDQS, TDQS#)	1.2	2.7	1.2	2.5	1.2	2.3	1.2	2.2	1.2	2.1	pF	1,2,3
CIO DDR3		1.2	2.5	1.2	2.3	1.2	2.2	1.2	2.1			pF	1,2,3
CCK	Input Capacitance (CK, CK#) CK#)	0.6	1.6	0.6	1.4	0.6	1.4	0.6	1.3	0.6	1.3	pF	2,3
CDCK	Input Capacitance Delta (CK, CK#)	0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
CDOS	Input/Output Capacitance Delta (DQS, DQS#)	0	0.2	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,5
CI	Input Capacitance (CTRL, ADD, CMD)	0.55	1.35	0.55	1.3	0.5 5	1.3	0.5 5	1.2	0.5 5	1.2	pF	2,3,6
CI DDR3		0.55	1.3	0.55	1.3	0.5 5	1.2	0.5 5	1.2			pF	2,3,6
CDI_CTRL	Input Capacitance Delta All CTRL Input Pins Pin	-0.5	0.3	-0.4	0.2	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
CDI_AD D_CMD	Input Capacitance Delta All ADD, CMD Input Pins Input Pins	-0.5	0.5	-0.4	0.4	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2,3,9,10

C _{DIO}	Input/Output Capacitance	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,1
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	Delta (DQ, DM, DQS, DQS#, TDQS, TDQS#)												1
CzQ	ZQ Input/Output Capacitance		3		3		3		3		3	pF	2,3,1 2

Note:

Note 1: Although the DM, TDQS, and TDQS# pins have different functions, the loading matches that of DQ and DQS.

Note 2: This parameter is not production tested; it is verified by design and characterization. Capacitance is measured according to JEP147 ("Procedure for Measuring Input Capacitance Using a Vector Network Analyzer (VNA)") with VDD, VDDQ, VSS, and VSSQ applied, all other pins floating (except the pin under test, CKE, RESET, and ODT when necessary). VDD = VDDQ = 1.5 V, VBIAS = VDD/2, and on-die termination is disabled.

Note 3: This parameter applies only to single-die; stacked/dual-chip devices are not included here. Note 4: Absolute value of CK - CK#.

Note 5: Absolute value of CIO(DQS) - CIO(DQS#).

Note 6: CI applies to ODT, CS#, CKE, A0-A15, BA0-BA2, RAS#, CAS#, and WE#.

Note 7: CDI_CTRL applies to ODT, CS#, and CKE.

Note 8: $CDI\_CTRL = CI(CTRL) - 0.5(CI(CLK) + CI(CLK\#)) \times$

Note 9: CDI_ADD_CMD applies to A0-A15, BA0-BA2, RAS#, CAS#, and WE#.

Note 10: $CDI\_ADD\_CMD = CI(ADD\_CMD) - 0.5(CI(CLK) + CI(CLK\#)) \times$

Note 11: $CDIO = CIO(DQ, DM) - 0.5(CIO(DQS) + CIO(DQS\#)) \times$

Note 12: Maximum external load capacitance on ZQ pin: 5 pF.

5.2.13 IDD Specifications and Measurement Conditions

IDD Specifications (DDR3)

Table 79 IDD Specification Information I

Abbrevia tion	Parameter	Bit Width	DDR3-1600 c11-11-11	DDR3-1866 13-13-13	DDR3-2133 14-14-14	Unit
IDD0	Operating Current0 One Bank Active -> Precharge	$\times 8$	100	120	130	mA
		$\times 16$	110	130	150	mA
IDD1	Operating Current1 One Bank Active ->	$\times 8$	110	125	135	mA

	Read -> Precharge	~~X~~ 16	120	135	155	mA
IDD2P0	Precharge Power Down Current Slow Exit – MR0 A12 = 0	~~X~~ 8	20	20	20	mA
		~~X~~ 16	22	22	22	mA
IDD2P1	Precharge Power Down Current Fast Exit – MR0 A12 = 1	~~X~~ 8	43	45	47	mA
		~~X~~ 16	45	47	47	mA
IDD2Q	Precharge Quiet Standby Current	8 ~~X~~	58	63	68	mA
		16 ~~X~~	60	65	70	mA
IDD2N	Precharge Standby Current	8 ~~X~~	61	66	71	mA
		16 ~~X~~	63	68	73	mA
IDD2NT	Precharge Standby ODT Current	8 ~~X~~	83	90	96	mA
		16 ~~X~~	85	92	98	mA
IDD3N	Active Standby Current	8 ~~X~~	88	96	100	mA
		16 ~~X~~	90	100	105	mA
IDD3P	Active Power-Down Current	8 ~~X~~	68	77	82	mA
		16 ~~X~~	70	80	85	mA
IDD4R	Operating Current Burst Read	8 ~~X~~	180	210	230	mA
		16 ~~X~~	190	220	240	mA
IDD4W	Operating Current Burst Write	8 ~~X~~	200	240	265	mA
		~~X~~ 16	210	250	280	mA
IDD5B	Burst Refresh Current	~~X~~ 8	170	185	200	mA
		~~X~~ 16	180	195	210	mA
IDD6	Self Refresh Current Normal Normal	~~X~~ 8	25	25	25	mA

		~~X~~ 16	25	25	25	mA
IDD6ET	Self Refresh Current Extended	~~X~~ 8	28	28	28	mA
		~~X~~ 16	28	28	28	mA
IDD7	All Bank Interleave Read Current	~~X~~ 8	220	255	275	mA
		~~X~~ 16	240	270	290	mA
IDD8	Reset Low Current	8 ~~X~~	21	21	22	mA
		16 ~~X~~	23	23	24	mA

Note:

1. Tc = 85°C; SRT and ASR are disabled.
2. Enabling ASR can increase IDDx by 2 mA.
3. Limited to Tc(MAX)=85°C.
4. Tc=85°C; ASR and ODT are disabled; SRT is enabled.
5. When Tc > +95 °C: All IDDx values must be increased by 30% over the 85 °C specification.
6. When Tc > +105 °C: All IDDx values must be increased by 50% over the 85 °C specification.
7. When Tc > 105°C, refresh is required; self-refresh mode is not available.

IDD Specifications (DDR3)

Table 80 IDD Specification Information II

Abbreviation	Parameter	Bit Width	DDR3-1600 c11-11-11	DDR3-1866 13-13-13	DDR3-2133 14-14-14	Unit
IDD0	Operating Current 0: One Bank Active -> Precharge Precharge	~~X~~ 8	100	120	130	mA
		~~X~~ 16	110	130	150	mA
IDD1	Operating Current1 One Bank Active ->	~~X~~ 8	110	125	135	mA
		~~X~~ 16	120	135	155	mA
	Read -> Precharge					
	Precharge Power Down Current Slow	~~X~~ 8	20	20	20	mA

IDD2P0	Exit – MRO A12 = 0	✕16	22	22	22	mA
IDD2P1	Precharge Power Down Current Fast Exit – MRO A12 = 1	✕8	43	45	47	mA
		16 ✕	45	47	47	mA
IDD2Q	Precharge Quiet Standby Current	8 ✕	58	63	68	mA
		16 ✕	60	65	70	mA
IDD2N	Precharge Standby Current	8 ✕	61	66	71	mA
		16 ✕	63	68	73	mA
IDD2NT	Precharge Standby ODT Current	8 ✕	83	90	96	mA
		16 ✕	85	92	98	mA
IDD3N	Active Standby Current	8 ✕	88	96	100	mA
		16 ✕	90	100	105	mA
IDD3P	Active Power Down Current Fast Exit Exit	8 ✕	68	77	82	mA
		16 ✕	70	80	85	mA
IDD4R	Operating Current Burst Read	8 ✕	180	210	230	mA
		16 ✕	190	220	240	mA
IDD4W	Operating Current Burst Write	✕8	200	240	265	mA
		✕16	210	250	280	mA
IDD5B	Burst Refresh Current	✕8	170	185	200	mA
		✕16	180	195	210	mA

IDD6	Self Refresh Current Normal	×8	25	25	25	mA
		×16	25	25	25	mA
IDD6ET	Self Refresh Current Extended	×8	28	28	28	mA
		×16	28	28	28	mA
IDD7	All Bank Interleave Read Current	×8	220	255	275	mA
		16 ×	240	270	290	mA
IDD8	Reset Low Current	8 ×	21	21	22	mA
		16 ×	23	23	24	mA

Note:

1. Tc = 85°C; SRT and ASR are disabled.
2. Enabling ASR can increase IDDx by 2 mA.
3. Limited to Tc(MAX)=85°C.
4. Tc=85°C; ASR and ODT are disabled; SRT is enabled.
5. When Tc>+105° C: All IDDx values must be derated (increased) by 30% from the 85°C specification.
6. When Tc>+105°C: All IDDx values must be derated (increased) by 50% from the 85°C specification.
7. When Tc>105°C: Self-refresh mode is not available; refresh is required.

5.2.13.1 IDD Measurement Conditions

Table 81 IDD Measurement Conditions Information

Abbreviation	Parameter
IDD0	Operating One Bank Active-Precharge Current; CKE: High; External Clock: On tCK, nRC, nRAS, CL: Refer to IDD and IDDQ timing tables; BL:8(1);AL:0; CS#: High during ACT and PRE clock cycles; Command, Address, Bank Address Inputs: Partially switching; Data IO: Mid-level DM: Maintained at 0; Bank Activity: Sequence of one bank activated at a time: 0,0,1,2,2,...; Output Buffer, RTT: Enabled in Mode Register MR2; ODT signal: held at 0;

IDD1	Operating One Bank Active-Read-Precharge Current CKE: High; External Clock: On tCK, tRC, tRAS, tRCD, CL: Refer to IDD and IDDQ timing tables; tCK, tRC, tRAS, tRCD, CL: See IDD and IDDQ timing tables; BL: 8 (BC: 4); AL: 0; CS#: HIGH during ACT, RD, and PRE clock cycles; Command, Address, Bank Address inputs, Data I/O: partially switching; Bank Activity: sequence activating one bank at a time: 0,0,1,2,2,...; Output Buffer, RTT: enabled in Mode Register MR2; ODT signal: held at 0;
IDD2N	Precharge Standby Current CKE: HIGH; Clock: ON tCK, CL: Refer to IDD and IDDQ timing tables; BL: 8 (1); AL: 0; CS#: HOLD HIGH; Command, Address, Bank Address inputs: partially switching; Data I/O: Hi-Z; DM: held LOW; Bank Activity: all banks closed; Output Buffer, RTT: Enabled in Mode Register MR2; ODT signal: held at 0;
IDD2P0	Precharge Power-Down Current Slow Exit CKE: High; Clock: On; tCK; CL: See IDD and IDDQ timing tables; BL: 8(1); AL: 0; CS#: maintained HIGH; Command, Address, Bank Address inputs: Held at 0; Data I/O: High-Z DM: Maintained at 0; Bank Activity: all banks closed; Output Buffer, RTT: Enabled in Mode Register MR2; ODT signal: held at 0; Precharge Power-Down Mode: Slow Exit (3)
IDD2P1	Precharge Power-Down Current Fast Exit CKE: HIGH; External clock: ON tCK; CL: See IDD and IDDQ Timing Table; BL: 8 (1); AL: 0; CS#: maintained HIGH; Command, Address, Bank Address inputs: HOLD LOW; Data IO: High-Z DM: Maintained at 0; Bank Activity: all banks closed; Output Buffer, RTT: Enabled in Mode Register MR2; ODT signal: held at 0; Precharge Power-Down Mode: Fast Exit (3)
IDD2Q	Precharge Quiet Standby Current

	CKE: High; External clock: enabled tCK, CL: See IDD and IDDQ timing tables; BL: 8 (1); AL: 0; CS#: maintained HIGH; Command, Address, Bank Address inputs: HOLD LOW; Data IO: High-Z DM: Maintained at 0; Bank Activity: all banks closed; Output Buffer, RTT: Enabled in Mode Register MR2; ODT signal: held at 0;
IDD3N	Active Standby Current CKE: HIGH; External Clock: ON tCK, CL: Refer to IDD and IDDQ timing tables; BL: 8 (1); AL: 0; CS#: HOLD HIGH; Command, Address, Bank Address inputs: partially toggled; Data IO: Mid-level (Hi-Z); DM: Held LOW; Bank Activity: All Banks Open; Output Buffer, RTT: Enabled in Mode Register MR2; ODT signal: held at 0;
IDD3P	Active Power-Down Current CKE: HIGH; External clock: ON tCK, CL: Refer to IDD and IDDQ timing tables; BL: 8 (1); AL: 0; CS#: HOLD HIGH; Command, Address, Bank Address inputs: HOLD LOW; Data IO: High-Z DM: Maintained at 0; Bank Activity: all banks closed; Output Buffer, RTT: Enabled in Mode Register MR2; ODT signal: held at 0;
IDD4R	Operating Burst Read Current CKE: High; External Clock: Enabled tCK, CL: Refer to IDD and IDDQ timing tables; BL: 8 (1,7); AL: 0; CS#: High during RD clock cycles; Command, Address, Bank Address inputs: partially toggled; Data IO: Seamless read data bursts with different data between one burst and the next burst; DM: Held at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2...; Output Buffer, RTT: enabled in mode register MR2; ODT signal: held at 0;
IDD4W	Operating Burst Write Current CKE: High; External Clock: Enabled

	tCK, CL: Refer to IDD and IDDQ timing tables; BL:8(1);AL:0; CS#: HIGH during RD clock cycles; Command, Address, Bank Address inputs: partially toggled; Data I/O: seamless write data burst with different data between bursts; DM: held LOW; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2...; Output Buffer, RTT: enabled in mode register MR2; ODT signal: held HIGH;
IDD5B	Burst Refresh Current CKE: HIGH; external clock: on tCK, CL, tRFC: Refer to IDD and IDDQ timing tables; BL:8(1);AL:0; CS#: High during REF clock cycle; Command, Address, Bank Address inputs: Partially toggling; Data I/O: Intermediate state DM: Maintained at 0; Bank Activity: REF command every tRFC clock cycle; Output Buffer and RTT: Enabled in mode register MR2; ODT signal: Maintained at 0;
IDD6	Self Refresh Current: Normal temperature range TCASE: 0 – 85 °C Auto Self Refresh(ASR):Disabled(4) Self Refresh Temperature Range (SRT): Normal (5) CKE: LOW; External clock: OFF CK, CK#: LOW CL: Refer to IDD and IDDQ timing tables; BL:8(1);AL:0; CS#, Data I/O, Command, Address, Bank Address inputs: Intermediate state; DM: Maintained at 0; Bank Activity:Self Refresh; Output Buffer, RTT: Enabled in Mode Register MR2; ODT signal: Mid-level;
IDD6ET	Self Refresh Current: Extended Temperature Range TCASE: 0 – 105 ° C Auto Self Refresh(ASR):Disabled(4) Self Refresh Temperature Range (SRT): Normal (5) CKE: LOW; External clock: OFF CK, CK#: LOW CL: Refer to IDD and IDDQ timing tables; BL:8(1);AL:0; CS#, Data IO, Command, Address, Bank Address inputs: Mid-level; DM: Maintained at 0; Bank Activity:Extended Self Refresh; Output Buffer, RTT: Enabled in Mode Register MR2;

	ODT signal: Mid-level;
IDD6TC	Auto Self-Refresh Current: (optional 6) TCASE: 0 – 105° C Auto Self Refresh (ASR): Enabled (4) Self Refresh Temperature Range (SRT): Normal (5) CKE: LOW; External clock: OFF CK, CK#: LOW CL: Refer to IDD and IDDQ timing tables; BL:8(1);AL:0; CS#, Data IO, Command, Address, Bank Address inputs: Mid-level; DM: Maintained at 0; Bank Activity: Self Refresh; Output Buffer, RTT: Enabled in Mode Register MR2; ODT signal: Mid-level;
IDD7	CKE: HIGH; External clock: OFF tCK, tRC, tRAS, tRCD, tFAW, CL: See IDD and IDDQ timing tables; BL:8(1,7);AL:CL-1; CS#: HIGH during ACT and RDA clock cycles; Data IO: Read data bursts with different data between one burst and the next; Command, Address, Bank Address inputs: Partially switching; DM: Maintained at 0; Bank Activity: Two interleaved cycles through banks with different addressing (0, 1, ...7); Output Buffer, RTT: Enabled in Mode Register MR1; ODT signal: held at 0;
IDD8	RESET Low Current RESET: low; External clock: off; CS#, Command, Address, Bank Address, Data IO: floating; ODT signal: floating Once power is stable and RESET has been low for at least 1 ms, the RESET low current reading is valid.

Note:

Burst length: fixed to BL8 by MRS, set MR0 A[1:0]=00B

Note 2 Output buffer enable: set MR1 A[12]=0B; set MR1 A[5,1]=01B; RTT_Nom enable: set MR1 A[9,6,2]=011B; RTT_Wr enable: set MR2 A[10,9]=10B

Precharge Power Down Mode: set MR0 A12=0B for slow exit or set MR0 A12=1B

for fast exit

Auto Self Refresh (ASR): set MR2 A6=0B disable, set 1B enable

Note 5 Self-refresh temperature range (SRT): Set MR2 A7=0B for normal temperature range, or set to 1B for extended temperature range

Note 6 Refer to the DRAM supplier's datasheet and/or DIMM SPD to determine whether the DDR3 SDRAM device supports optional features or

requirements.

Note 7 Read burst type: Nibble Sequential, set MR0 A[3]=0B

5.2.13.2 IDD0 Measurement Loop Pattern

CK#	CK#	Sub_Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	ACT	0	0	1	1	0	0	0	0	0	0	0	0	-
		1,2	D,D	1	0	0	0	0	0	0	0	0	0	0	0	-
		3,4	0,0	1	1	1	1	0	0	0	0	0	0	0	0	-
		...	repeat pattern 1...4 until nRAS-1, truncate if necessary													
		nRAS	PRE	0	0	0	1	0	0	0	0	0	0	0	0	-
		...	repeat pattern 1...4 until nRC-1, truncate if necessary													
		1*nRC+0	ACT	0	0	1	1	0	0	0	0	0	0	F	0	-
		1*nRC+1,2	D,D	1	0	0	0	0	0	0	0	0	0	F	0	-
		1*nRC+3,4	D#,D#	1	1	1	1	0	0	0	0	0	0	F	0	-
		...	repeat pattern nRC+1...4 until 1*nRC-1+nRAS, truncate if necessary													
		1*nRC+nRAS	PRE	0	0	0	1	0	0	0	0	0	0	F	0	-
		...	repeat pattern nRC+1...4 until 2*nRC-1, truncate if necessary													
		2*nRC	repeat Sub_Loop 0, use BA[2:0]=1 instead													
		4*nRC	repeat Sub_Loop 0, use BA[2:0]=2 instead													
		6*nRC	repeat Sub_Loop 0, use BA[2:0]=3 instead													
		8*nRC	repeat Sub_Loop 0, use BA[2:0]=4 instead													
		10*nRC	repeat Sub_Loop 0 with BA[2:0]=5													
		12*nRC	repeat Sub_Loop 0 with BA[2:0]=6													
		14*nRC	repeat Sub_Loop 0 with BA[2:0]=7													

Note:

Notes:

1. DM must be driven low at all times. DQS and DQS# are high impedance.
2. DQ signals are high impedance.

5.2.13.3 IDD1 Measurement Loop Mode

Table 83 IDD1 Measurement Loop Mode Information

Data	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A[2:0]	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A[6:3]	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A[9:7]	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A[10]	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A[15:11]	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BA[2:0]	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ODT	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
WE#	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CAS#	-	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RAS#	-	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CS#	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Command	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Cycle Number	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Sub_Loop	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CKE	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
, CK CK#	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Static High																
0																
1,2																
3,4																
D#,D#																
repeat pattern 1...4 until nRCD-1, truncate if necessary																
nRAS																
PRE																
repeat pattern 1...4 until nRAS-1, truncate if necessary																
1*nRC+0																
ACT																
1*nRC+1,2																
D,D																
1*nRC+3,4																
D#,D#																
repeat patterns 1-4 from nRC+1 until nRC-1+nRCD, truncating if necessary																
1*nRC+nRAS																
PRE																
repeat pattern nRC+1 to nRC+4 until nRC+nRAS-1, truncate if necessary																
2*nRC																
repeat Sub_Loop 0, use BA[2:0]=1 instead																
4*nRC																
repeat Sub_Loop 0, use BA[2:0]=2 instead																
6*nRC																
repeat Sub_Loop 0, use BA[2:0]=3 instead																
8*nRC																
repeat Sub_Loop 0, use BA[2:0]=4 instead																
10*nRC																
repeat Sub_Loop 0, use BA[2:0]=5 instead																
12*nRC																
repeat Sub_Loop 0, use BA[2:0]=6 instead																
14*nRC																
repeat Sub_Loop 0, use BA[2:0]=7 instead																

Note:

- DM must be driven low at all times. DQS and DQS# are high impedance.
- A burst sequence is driven on each DQ signal by a read command. The DQ signals are high impedance outside of burst operations.

5.2.13.4 IDD2N and IDD3N Measurement Loop Mode

Data	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A[2:0]	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A[6:3]	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A[9:7]	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A[10]	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A[15:11]	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BA[2:0]	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ODT	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
WE#	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CAS#	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RAS#	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CS#	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Command	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Cycle Number	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Sub_Loop	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CKE	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
, CK CK#	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Static High																
0																
1																

			2	D#	1	1	1	1	0	0	0	0	0	F	0	-
			3	D#	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub_Loop 0, use BA[2:0]=1 instead												
		2	8-11	repeat Sub_Loop 0, use BA[2:0]=2 instead												
		3	12-15	repeat Sub_Loop 0, use BA[2:0]=3 instead												
		4	16-19	repeat Sub_Loop 0, use BA[2:0]=4 instead												
		5	20-23	repeat Sub_Loop 0, use BA[2:0]=5 instead												
		6	24-27	repeat Sub_Loop 0, use BA[2:0]=6 instead												
		7	28-31	repeat Sub_Loop 0, use BA[2:0]=7 instead												

Note:

1. DM must always be low. DQS and DQS# are in the intermediate state.
2. DQ signals are in high-impedance state.

5.2.13.5 IDD4R and IDDQ4R Measurement Loop Pattern

T _{CK} h _{lo}	CK#	Sub_Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
toggling	Static High	0	0	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2,3	D#,D#	1	1	1	1	0	0	0	0	0	0	0	-
			4	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	0	0	0	F	0	-
			6,7	D#,D#	1	1	1	1	0	0	0	0	0	F	0	-
		1	8-15	repeat Sub-loop 0, but BA[2:0]=1 instead												
		2	16-23	repeat Sub-loop 0, but BA[2:0]=2 instead												
		3	24-31	repeat Sub-loop 0, but BA[2:0]=3 instead												
		4	32-39	repeat Sub-loop 0, but BA[2:0]=4 instead												
		5	40-47	repeat Sub-loop 0, but BA[2:0]=5 instead												
		6	48-55	repeat Sub_Loop 0, but BA[2:0]=6 instead												
		7	56-63	repeat Sub_Loop 0, but BA[2:0]=7 instead												

Note:

1. DM must always be driven low. DQS, DQS# are used according to the RD command; otherwise, they are tristate.
2. Burst sequence driven on each DQ signal by a read command. Outside burst operation, DQ signals are tristate.

5.2.13.6 IDD4W Measurement Loop Pattern

Data	A[2:0]	A[6:3]	A[9:7]	A[10]	A[15:11]	BA[2:0]	ODT	WE#	CAS#	RAS#	CS#	Command	Cycle Number	Sub_Loop	CKE	T _{clk} h ₁₂ CK#	
00000000	0	0	0	0	0	0	1	0	0	0	1	WR	0	0	Static High	toggling	
-	0	0	0	0	0	0	1	0	0	0	1	D	1				
-	0	0	0	0	0	0	1	1	1	1	1	D#,D#	2,3				
00110011	0	F	0	0	0	0	1	0	0	1	0	WR	4				
-	0	F	0	0	0	0	1	0	0	0	1	D	5				
-	0	F	0	0	0	0	1	1	1	1	1	D#,D#	6,7				
repeat Sub_Loop 0, but BA[2:0]=1 instead														1			8-15
repeat Sub_Loop 0, but BA[2:0]=2 instead														2			16-23
repeat Sub_Loop 0, but BA[2:0]=3 instead														3			24-31
repeat Sub_Loop 0, but BA[2:0]=4 instead														4			32-39
repeat Sub_Loop 0, but BA[2:0]=5 instead														5			40-47
repeat Sub_Loop 0, but BA[2:0]=6 instead														6			48-55
repeat Sub_Loop 0, but BA[2:0]=7 instead														7			56-63

Note:

1. DM must always be driven low. DQS, DQS# are used according to the WR command; otherwise, they are tristate.
2. Burst sequence driven on each DQ signal by write command. Outside burst operation, DQ signals are in high-impedance state.

5.2.13.7 IDD5B Measurement Loop Pattern

Data	A[2:0]	A[6:3]	A[9:7]	A[10]	A[15:11]	BA[2:0]	ODT	WE#	CAS#	RAS#	CS#	Command	Cycle Number	Sub_Loop	CKE	T _{clk} h ₁₂ CK#
-	0	0	0	0	0	0	0	1	0	0	0	REF	0	0	0	gll

1	1,2	D,D	1	0	0	0	0	0	0	0	0	0	0	-
	3,4	D#,D#	1	1	1	1	0	0	0	0	0	F	0	-
	5-8	repeat cycles1-4, but BA[2:0]=1												
	9-12	repeat cycles1-4, but BA[2:0]=2												
	13-16	repeat cycles1-4, but BA[2:0]=3												
	17-20	repeat cycles1-4, but BA[2:0]=4												
	21-24	repeat cycles1-4, but BA[2:0]=5												
	25-28	repeat cycles1-4, but BA[2:0]=6												
	29-32	repeat cycles1-4, but BA[2:0]=7												
	2	33-nRFC-1	repeat Sub_Loop1,until nRFC-1,Truncate if necessary											

Note:

1. DM must be held LOW. DQS, DQS# are in high-impedance state.
2. DQ signals are in high-impedance state.

5.2.13.8 IDD7 Measurement Loop Pattern

Note: Sub_Loop10-19 have the opposite A[6:3] pattern and data pattern compared to Sub_Loop0-9.

CK nla	CK#	CKE	Sub_Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
toggling		Static High	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	-
				1	RDA	0	1	0	1	0	0	1	0	0	0	0	0000000 0
				2	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	...	repeat above D command until nRRD-1												
				nRRD	ACT	0	0	1	1	0	1	0	0	0	F	0	-
				nRRD+1	RDA	0	1	0	1	0	1	1	0	0	F	0	0011001 1
				nRRD+2	D	1	0	0	0	0	1	0	0	0	F	0	-
				...	repeat above D command until nRRD-1												
			4	2	2*nRRD	repeat Sub_Loop0, but BA[2:0]=2											
				3	3*nRRD	repeat Sub_Loop0, but BA[2:0]=3											
				4	4*nRRD	D	1	0	0	0	3	0	0	0	F	0	-
				...	Assert and repeat the above D command until nFAW-1, if necessary.												
			5	nFAW	repeat Sub_Loop0, but BA[2:0]=4												

6	nFAW+nRRD	repeat Sub_Loop0, but BA[2:0]=5													
7	nFAW+2*nRRD	repeat Sub_Loop0, but BA[2:0]=6													
8	nFAW+3*nRRD	repeat Sub_Loop0, but BA[2:0]=7													
9	nFAW+4*nRRD	D	1	0	0	0	0	7	0	0	0	F	0	-	
		Assert and repeat above D command until 2*nFAW-1, if necessary													
10	2*nFAW+0	AC T	0	0	1	1	0	0	0	0	0	F	0	-	
	2*nFAW+1	RD A	0	1	0	1	0	0	0	1	0	F	0	0011001 1	
	2*nFAW+2	D	1	0	0	0	0	0	0	0	0	F	0	-	
		Assert and repeat above D command until 2*nFAW+nRRD-1													
11	2*nFAW+nRRD +1	AC T	0	0	1	1	0	1	0	0	0	0	0	-	
	2*nFAW+nRRD +2	RD A	0	1	0	1	0	1	0	1	0	0	0	0011001 1	
	2*nFAW+nRRD +3	D	1	0	0	0	0	1	0	0	0	0	0	-	
		Assert and repeat above D command until 2*nFAW+nRRD-1													
12	2*nFAW+2*nRRD RD	repeat Sub_Loop10, but BA[2:0]=2													
13	2*nFAW+3*nRRD RD	repeat Sub_Loop11, but BA[2:0]=3													
14	2*nFAW+4*nRRD RD	D	1	0	0	0	0	3	0	0	0	0	0	-	
		Assert and repeat above D command until 3*nFAW-1, if necessary													
15	3*nFAW	repeat Sub_Loop10, but BA[2:0]=4													
16	3*nFAW+nRRD	repeat Sub_Loop11, but BA[2:0]=5													
17	3*nFAW+2*nRRD RD	repeat Sub_Loop10, but BA[2:0]=6													
18	3*nFAW+3*nRRD RD	repeat Sub_Loop11, but BA[2:0]=7													
19	3*nFAW+4*nRRD RD	D	1	0	0	0	0	7	0	0	0	0	0	-	
		Assert and repeat above D command until 4*nFAW-1, if necessary													

Note:

1. DM must be held LOW (may be active during write operations). DQS, DQS# are used based on read command, otherwise at mid-level.
2. Burst sequence driven on each DQ signal by a read command. Outside of burst operations, DQ signals are at mid-level.

Speed Bin

DDR3-2133:

Table 89 DDR3-2133 Timing Parameters

Speed Bin			DDR3-2133		Unit
CL-nRCD-nRP			14-14-14		
Parameter			Min	Max	
tAA			13.09	20	ns
tRCD			13.09	-	ns
tRP			13.09	-	ns
rRAS			33	9XtREFI	ns
tRC			40.09	-	ns
tCK(avg)	CL=5	CWL=5	Reserve		ns
		CWL=6/7/8/9/10	Reserve		ns
	CL=14	CWL=5	2.5	3.3	ns
		CWL=9	Reserve		ns
		CWL=9/10/11/12	Reserve		ns
	CL=14	CWL=5	1.875	<2.5	ns
		CWL=6	Reserve		ns
		CWL=9	Reserve		ns
		CWL=9/10/11	Reserve		ns
	CL=14	CWL=5	1.875	<2.5	ns
		CWL=6	Reserve		ns
		CWL=7	Reserve		ns
		CWL=8/9/10	Reserve		ns
	CL=14	CWL=5/6	Reserve		ns
		CWL=7	1.5	<1.875	ns
		CWL=8	Reserve		ns
		CWL=9/10	Reserve		ns
	CL=10	CWL=5/6	Reserve		ns
		CWL=7	1.5	<1.875	ns
		CWL=8	Reserve		ns
		CWL=9	Reserve		ns
		CWL=10	Reserve		ns
	CL=11	CWL=5/6/7	Reserve		ns
		CWL=8	1.25	<1.5	ns
		CWL=9	Reserve		ns
		CWL=10	Reserve		ns
	CL=12	CWL=5/6/7/8	Reserve		ns
		CWL=9	Reserve		ns
		CWL=10	Reserve		ns
	CL=13	CWL=5/6/7/8	Reserve		ns
		CWL=9	1.07	<1.25	ns
		CWL=10	Reserve		ns
	CL=14	CWL=5/6/7/8/9	Reserve		ns
		CWL=10	0.938	<1.07	ns
Support CL 5,6,7,8,9,10,11,12,13,14			5,6,7,8,9,10,11,13,14		nCK
Support CWL			5,6,7,8,9,10		nCK

DDR3-1866 and DDR3L-1866:

Table 90 DDR3(L)-1866 Timing Parameters

Speed Bin			DDR3(L)-1866		Unit
CL-nRCD-nRP			13-13-13		
Parameter			Min	Max	
tAA			13.91	20	ns
tRCD			13.91	-	ns
tRP			13.91	-	ns
rRAS			34	9XtREFI	ns
tRC			47.91	-	ns
tCK(Avg)	CL=5	CWL=5	Reserve		ns
		CWL=6/7/8/9	Reserve		ns
	CL=6	CWL=5	2.5	3.3	ns
		CWL=6	Reserve		ns
		CWL=7/8/9	Reserve		ns
	CL=7	CWL=5	1.875	<2.5	ns
		CWL=6	Reserve		ns
		CWL=7	Reserve		ns
		CWL=8/9	Reserve		ns
	CL=8	CWL=5	1.875	<2.5	ns
		CWL=6	Reserve		ns
		CWL=7	Reserve		ns
		CWL=8/9	Reserve		ns
	CL=9	CWL=5/6	Reserve		ns
		CWL=7	1.5	<1.875	ns
		CWL=8	Reserve		ns
		CWL=9	Reserve		ns
	CL=10	CWL=5/6	Reserve		ns
		CWL=7	1.5	<1.875	ns
		CWL=8	Reserve		ns
		CWL=9	Reserve		ns
	CL=11	CWL=5/6/7	Reserve		ns
		CWL=8	1.25	<1.5	ns
		CWL=9	Reserve		ns
	CL=12	CWL=5/6/7/8	Reserve		ns
		CWL=9	Reserve		ns
	CL=13	CWL=5/6/7/8	Reserve		ns
		CWL=9	1.07	<1.25	ns
Support CL			5,6,7,8,9,10,11,13		nCK
Support CWL			5,6,7,8,9		nCK

DDR3-1600 and DDR3L-1600:

Table 91 DDR3(L)-1600 Timing Parameters

Speed Bin			DDR3(L)-1600		Unit
CL-nRCD-nRP			11-11-11		
Parameter			Min	Max	
tAA			13.75	20	ns
tRCD			13.75	-	ns
tRP			13.75	-	ns
rRAS			35	9XtREFI	ns
tRC			48.75	-	ns
tCK(Avg)	CL=5	CWL=5	3	3.3	ns
		CWL=6/7/8	Reserve		ns
	CL=6	CWL=5	2.5	3.3	ns
		CWL=6	Reserve		ns
		CWL=7/8	Reserve		ns
	CL=7	CWL=5	Reserve		ns
		CWL=6	1.875	<2.5	ns
		CWL=7	Reserve		ns
		CWL=8	Reserve		ns
	CL=8	CWL=5	Reserve		ns
		CWL=6	1.875	<2.5	ns
		CWL=7	Reserve		ns
		CWL=8	Reserve		ns
	CL=9	CWL=5/6	Reserve		ns
		CWL=7	1.5	<1.875	ns
		CWL=8	Reserve		ns
	CL=10	CWL=5/6	Reserve		ns
		CWL=7	1.5	<1.875	ns
		CWL=8	Reserve		ns
	CL=11	CWL=5/6/7	Reserve		ns
		CWL=8	1.25	<1.5	ns
Support CL			5,6,7,8,9,10,11		nCK
Support CWL			5,6,7,8		nCK

DDR3-1333 and DDR3L-1333:

Table 92 DDR3(L)-1333 Timing Parameters

Speed Bin	DDR3(L)-1333		DDR3-1333		Unit
CL-nRCD-nRP	9-9-9		10-10-10		
Parameter	Min	Max	Min	Max	
tAA	13.5	20	15	20	ns
tRCD	13.5	-	15	-	ns
tRP	13.5	-	15	-	ns
rRAS	36	9XtREFI	36	9XtREFI	ns
tRC	49.5	-	51	-	ns

tCK(Avg)	CL=5	CWL=5	3	3.3	3	3.3	ns	
		CWL=6	Reserve			Reserve		ns
		CWL=7	Reserve			Reserve		
	CL=6	CWL=5	2.5	3.3	2.5	3.3	ns	
		CWL=6	Reserve			Reserve		ns
		CWL=7	Reserve			Reserve		ns
	CL=7	CWL=5	Reserve			Reserve		ns
		CWL=6	1.875	<2.5	Reserve		ns	
		CWL=7	Reserve			Reserve		ns
	CL=8	CWL=5	Reserve			Reserve		ns
		CWL=6	1.875	<2.5	1.875	<2.5	ns	
		CWL=7	Reserve			Reserve		ns
	CL=9	CWL=5	Reserve			Reserve		ns
		CWL=6	Reserve			Reserve		ns
		CWL7	1.5	<1.875	Reserve		ns	
	CL=10	CWL=5	Reserve			Reserve		ns
		CWL=6	Reserve			Reserve		ns
		CWL=7	1.5	<1.875	1.5	<1.875	ns	
Support CL			5,6,7,8,9,(10)			5,6,8,(10)		nCK
Support CWL			5,6,7			5,6,7		nCK

DDR3-1066 and DDR3L-1066:

Table 93 DDR3(L)-1066 Timing Parameters

Speed Bin			DDR3(L)-1066		DDR3-1066		Unit
CL-nRCD-nRP			7-7-7		8-8-8		
Parameter			Min	Max	Min	Max	
tAA			13.125	20	15	20	ns
tRCD			13.125	-	15	-	ns
tRP			13.125	-	15	-	ns
rRAS			37.5	9XtREFI	37.5	9XtREFI	ns
tRC			50.625	-	52.5	-	ns
tCK(Avg)	CL=5	CWL=5	3	3.3	3	3.3	ns
		CWL=6	Reserve		Reserve		ns
	CL=6	CWL=5	2.5	3.3	2.5	3.3	ns
		CWL=6	Reserve		Reserve		ns
	CL=7	CWL=5	Reserve		Reserve		ns
		CWL=6	1.875	<2.5	Reserve		ns
	CL=8	CWL=5	Reserve		Reserve		ns
		CWL=6	1.875	<2.5	1.875	<2.5	ns
Support CL			5,6,7,8		5,6,8		nCK
Support CWL			5,6		5,6		nCK

Note:

Note 1 CL setting and CWL setting define the requirements for tCK(AVG).min and tCK(AVG).max. When selecting tCK(AVG), the requirements of both CL setting and CWL setting must be satisfied.

Note 2 tCK(AVG).min limitation: Since CAS latency is not a pure analog quantity, data and strobe output signals are synchronized via the DLL. The DLL may not guarantee reliable operation at all intermediate frequencies. The application should use the next larger JEDEC standard tCK(AVG) value.

(3.0, 2.5, 1.875, 1.5, 1.25, 1.07 or 0.938 ns), when calculating $CL[nCK] = tAA[ns] / tCK(AVG)[ns]$, round up to the next 'supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.

Note 3 tCK(AVG).max limit: Calculate $tCK(AVG).max = tAA(min)/CL\ SELECTED$ and round down to the next valid interval.

(e.g., 3.3ns, 2.5ns, 1.875ns, 1.5ns, 1.25ns, 1.07ns, or 0.938ns). This result is the tCK(AVG).max corresponding to CL SELECTED.

Note 4 Reserved settings are not allowed. The user must program a different value.

Note 5 Optional settings allow certain devices in the industry to support this setting, but it is not a mandatory feature. For information on whether and how this setting is supported, refer to the supplier's datasheet and/or DIMM SPD information.

Note 6 Any DDR3-1066 speed also supports functional operation at lower frequencies, as shown in the table. These frequencies are not production tested but are design/characterization verified.

Note 7 Any DDR3-1333 speed also supports functional operation at lower frequencies, as shown in the table. These frequencies are not production tested but are design/characterization verified.

Note 8 Any DDR3-1600 speed also supports functional operation at lower frequencies, as shown in the table. These frequencies are not production tested but are design/characterization verified.

Note 9 Any DDR3-1866 speed also supports functional operation at lower frequencies, as shown in the table. These frequencies are not production tested but are design/characterization verified.

Note 10 Any DDR3-2133 speed also supports functional operation at the lower frequencies shown in the table; these frequencies are not production tested but are verified by design/characterization.

Note 11 For devices supporting optional down to CL=7 and CL=9, tAamin, tRCDmin, and tRPmin must be 13.125 ns. The SPD must be programmed accordingly. For example, a DDR3-1333 (9-9-9) device supporting down to 1066 (7-7-7) should program SPD bytes tAamin (byte 16), tRCDmin (byte 18), and tRPmin (byte 20) to 13.125 ns. A DDR3-1600 (11-11-11) device supporting down to DDR3-1333 (9-9-9) or DDR3-1066 (7-7-7) should program SPD bytes tAamin (byte 16), tRCDmin (byte 18), and tRPmin

(byte 20) to 13.125 ns. Once tRP (byte 20) is programmed to 13.125 ns, tRCmin (bytes 21, 23) should also be programmed accordingly. For example, DDR3-1333 (9-9-9) is 49.125 ns (tRASmin + tRPmin = 36 ns + 13.125 ns), DDR3-1600 (11-11-11) is

48.125 ns (tRASmin + tRPmin = 35 ns + 13.125 ns).

Note 12 If the DRAM data rate is lower than 800 MT/s, DDR3 800 AC timing applies.

Note 13 For CL5 support, refer to DIMM SPD information. The DRAM must support CL5. CL5 is not mandatory in SPD encoding. Note 14 For devices supporting optional down to CL=11, CL=9, and CL=7, tAA/tRCD/tRPmin must be 13.125 ns. The SPD settings must be programmed to match. For example, a DDR3-1866 (13-13-13) device supporting down bin to DDR3-1600 (11-11-11), DDR3-1333 (9-9-9), or 1066 (7-7-7) should program SPD bytes tAAmin (byte 16), tRCDmin (byte 18), and tRPmin (byte 20) to 13.125 ns. Once tRP (byte 20) is programmed to 13.125 ns, tRCmin (bytes 21, 23) should also be programmed accordingly. For example, 47.125 ns (tRASmin + tRPmin = 34 ns + 13.125 ns).

5.2.13.9 Electrical Characteristics and AC Timing

Speed Bin (DDR3(L)-1066) Timing Parameters

Table 94 DDR3-1066(L) Timing Parameters I

Parameter	Abbreviation	DDR3-1066(L)		Unit	Notes
		Min	Max		
Clock Timng					
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	ns	
Average Clock Period	tCK(avg)	Reference Speed Bin		ps	
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min tCK(avg)max + tJIT(per)max		ps	
Absolute high pulse width	tCH(abs)	0.43	-	tCK(avg)	
Absolute Low Pulse Width	tCL(abs)	0.43	-	tCK(avg)	
Clock Period Jitter	tJIT(per)	-90	90	ps	
Clock Period Jitter during DLL Locking Period	tJIT(per,lck)	-80	80	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	180		ps	
Cycle to Cycle Period Jitter during DLL locking Period	tJIT(cc, lk)	160		ps	
Duty Cycle Jitter	tJIT(duty)	-	-	ps	
Cumulative error across n = 13,14...49,50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68 ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68 ln(n)) * tJIT(per)max		Ps	
Data Timing					
DQS, DQS# to DQ skew, per group, pre access	tDQSQ	-	150	ps	
DQ output hold time from DQS,DQS#	tQH	0.38	-	tCK(avg)	
DQ low impedance time from CK, CK#	tLZ(DQ)	-600	300	ps	
DQ high impedance time	tHZ(DQ)	-	300	ps	

from CK,CK#					
Data setup time to DQS,DQS# reference to VIH(ac)/VIL(ac) levels	tDS(base) DDR3-AC175	25	-	ps	
	tDS(base) DDR3-AC150	75	-	ps	
	tDS(base) DDR3-AC160	40	-	ps	
	tDS(base) DDR3-AC135	90	-	ps	
Data hold time to DQS,DQS# reference to VIH(ac)/VIL(ac) levels	tDS(base) DDR3-DC100	100	-	ps	
	tDS(base) DDR3-DC90	110	-	ps	
DQ and DM Input pulsewidth for each input	tDIPW	490	-	ps	

Table 95 DDR3-1066(L) Timing Parameters II

Parameter	Abbreviation	DDR3-1066(L)		Unit	Notes
		Min	Max		
Data Strobe Timing					
DQS,DQS# differential Read Preamble	tRPRE	0.9	Note 19	tCK(avg)	
DQS,DQS# differential Read Postamble	tRPST	0.3	Note 11	tCK(avg)	
DQS,DQS# differential output high time	tDQH	0.38	-	tCK(avg)	
DQS,DQS# differential output low time	tDQL	0.38	-	tCK(avg)	
DQS, DQS# differential write preamble	tWPRE	0.9	-	tCK(avg)	
DQS, DQS# differential write postamble	tWPST	0.3	-	tCK(avg)	
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-300	300	ps	
DQS, DQS# low-impedance time (Referenced from RL-1)	tLZ(DQS)	-600	300	ps	
DQS, DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	300	ps	
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	tCK(avg)	
DQS,DQS# differential input high pulse width	tDQSH	0.45	0.55	tCK(avg)	
DQS,DQS# rising edge to CK,CK# rising edge	tDQSS	-0.25	0.25	tCK(avg)	
DQS,DQS# falling edge setup time to CK,CK# rising edge	tDSS	0.2	-	tCK(avg)	
DQS,DQS# falling edge hold time to CK,CK# rising edge	tDHS	0.2	-	tCK(avg)	
Command and Address Timing					
DLL locking time	tDLLK	512	-	nCK	
Internal READ Command to Precharge Command delay	tRTP	max(4nCK,7.5ns)	-		

Delay from start of internal write transaction to internal read command	tWTR	max(4nCK,7.5ns)	-		
Write recovery time	tWR	15	-	ns	
Mode Register Set Command cycle time	tMRD	4	-	nCK	
Mode Register Set Command update delay	tMOD	max(12nCK,15ns)	-		
ACT to internal read or write delay time	tRCD	See Speed Bin			
PRE Command period	tRP				
ACT to ACT or PRE command period	tRC				
Active to Precharge command period	tRAS				
CAS# to CAS# command delay	tCCD	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR+round(tRP/tCK(avg))		nCK	

Table 96 DDR3-1066(L) Timing Parameter Table III

Parameter	Abbreviation	DDR3-1066(L)		Unit	Notes
		Min	Max		
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK	
Active to Active command period for 1KB page size	tRRD	max(4nCK,7.5ns)	-		
Active to Active command period for 2KB page size	tRRD	max(4nCK,10ns)	-		
Four activate window for 1KB page size	tFAW	37.5	-	ns	
Four activate window for 2KB page size	tFAW	50	-	ns	
Command and Address setup time to CK,CK# reference to VIH(ac)/VIL(ac) levels	tIS(Base)DDR3-AC175	125	-	ps	
	tIS(Base)DDR3-AC150	275	-	ns	
	tIS(Base)	140	-	ps	
	tIS(Base)	290	-	ns	
Command and Address hold time referenced to CK, CK# with respect to VIH(ac)/VIL(ac) levels	tIH(Base)DDR3-DC100	200	-	ns	
	tIH(Base)DDR3-DC90	210	-	ns	
Command and Address input pulse width each input	tIPW	780	-	ps	
Calibration Timing					
Power-up and RESET calibration time	tZQinit	tZQinit(min): max(512 tCK, 640 ns) tZQinit(max): -		nCK	
Normal operation Full calibration time	tZQoper	tZQoper(min): max(256 tCK, 320 ns) tZQoper(max): -		nCK	
Normal operation Short calibration time	tZQCS	tZQCS(min): max(64 tCK, 80 ns) tZQCSmax:-		nCK	
Reset Timing					
Exit Reset from CKE high to a valid command command	tXRP	max(5nCK,tRFC(min))+10ns)		-	
Self Refresh Timing					
Exit Self Refresh to commands not requiring a Locked DLL requiring a Locked DLL	tXS	max(5nCK,tRFC(min))+10ns)		-	
Exit Self Refresh to commands requiring a Locked DLL requiring a Locked DLL	tXSDLL	tDLLK (min)		-	nCK
Minimum CKE low width for Self Refresh Self Refresh entry to Exit timing	tCKSER	tCKE(min) + 1 nCK		-	

Valid Clock Requirement after Self Refresh	tCKSRE	max(5 nCK, 10 ns)	-		
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Refresh entry (SRE) or Power Down Entry Entry (PDE)					
Valid clock requirement before self-refresh exit Self-refresh exit (SRX), power-down exit (PDX), or Reset exit	tCKSRX	max(5nCK,10ns)	-		

Table 97 DDR3-1066(L) Timing Parameter Table IV

Parameter	Abbreviation	DDR3-1066(L)		Unit	Notes
		Min	Max		
Power Down Timing					
Exit power-down to any valid command with DLL enabled; exit precharge power-down (DLL frozen) to command not requiring a locked DLL not requiring a locked DLL	tXP	max(3nCK,7.5ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL Locked DLL	tXDLL	max(10nCK,24ns)	-		
CKE minimum pulse width	tCKE	max(3nCK,5.625ns)	-		
Command pass disable delay	tCPDED	1	-	nCK	
Power Down Entry to Exit Timing	tPD	tCK(min)	9*tREFI		
Timing of ACT command to PowerDown entry PowerDown entry	tACTPDEN	1	-	nCK	
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	nCK	
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK	
Timing of WR command to Power Down entry(BL8OTF,BL8MRS,BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	nCK	
Timing of WRA command to Power PowerDown entry(BL8OTF,BL8MRS,BC4OTF)	tWRPADEN	WL+4+WR+1	-	nCK	
Timing of WR command to PowerDown entry(BC4MRS) Down entry(BC4MRS)	tWRPDEN	WL+2+(tWR/tCK(avg))	-	nCK	
Timing of WRA command to Power Down entry(BC4MRS)	tWRPADEN	WL+2+WR+1	-	nCK	
Timing of REF command to PowerDown entry Down entry	tREFPDEN	1	-	nCK	
Timing of MRS command to PowerDown entry Down entry	tMRSPDEN	tMRSPDEN(min)	-		
ODT Timing					
ODT turn-on Latency	ODTLon	WL-2=CWL+AL-2	-	nCK	
ODT turn-off Latency	ODTLoff	WL-2=CWL+AL-2	-	nCK	

ODT high time without write command command or with write command and	ODTH4	4	-	nCK	
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BC4						
ODT high time with write command and BL8 and BL8	ODTH8	8	-	nCK		
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	ns		
Asynchronous RTT turn-off delay (Power Down with DLL frozen)	tAOFPD	2	8.5	ns		
RTT turn-on	tAON	-300	300	ps		
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	tCK(avg)		
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)		
Parameter		Abbreviation	DDR3-1066(L)		Unit	Notes
			Min	Max		
Write Leveling Timing						
First DQS/DQS# rising edge after write leveling mode is programmed is programmed	tWLMRD	40	-	nCK		
DQS/DQS# delay after write leveling mode is programmed programmed	tWLDQSEN	25	-	nCK		
Write Leveling setup time from rising CK/CK# crossing to rising DQS/DQS# crossing	tWLS	245	-	ps		
Write Leveling hold time from rising DQS/DQS# rising CK, CK# crossing	tCPDED	245	-	ps		
Write Leveling Output Delay	tWLO	0	9	ns		
Write Leveling Output Error	tWLOE	0	2	ns		

Speed Bin (DDR3(L)-1333) Timing Parameters

Table 98 DDR3-1333(L) Timing Parameters Table I

Parameter	Abbreviation	DDR3-1333(L)		Unit	Notes
		Min	Max		
Clock Timig					
Minimum Clock Cycle Time(DLL off mode)	tCK(DLL_OFF)	8	-	ns	
Average Clock Period	tCK(avg)	Reference Speed Bin		ps	
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)	
Absolute Clock Period	tCK(abs)	min:tCK(avg)min+tJIT(per)min max:tCK(avg)max+tJIT(per)max		ps	
Absolute high pulse width	tCH(abs)	0.43	-	tCK(avg)	
Absolute low pulse width	tCL(abs)	0.43	-	tCK(avg)	
Clock Period Jitter	tJIT(per)	-80	80	ps	
Clock Period Jitter during DLL Locking Period Locking Period	tJIT(per,lck)	-70	70	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	160		ps	

Cycle to Cycle Period Jitter during DLL locking Period	tJIT(cc,lck)	140		ps	
Duty Cycle Jitter	tJIT(duty)	-	-	ps	
Cumulative Error across n = 13, 14, ..., 49, 50 cycles	tERR(nper)	tERR(nper)min=(1+0.68ln(n))*tJIT(per)min; tERR(nper)max=(1+0.68ln(n))*tJIT(per)max		ps	
Data Timg					
DQS,DQS# to DQ skew,per group,pre access	tDQSQ	-	125	ps	
DQ output hold time from DQS,DQS#	tQH	0.38	-	tCK(avg)	
DQ low impedance time from CK,CK#	tLZ(DQ)	-500	250	ps	
DQ high impedance time from CK,CK#	tHZ(DQ)	-	250	ps	
Data setup time to DQS,DQS# reference to VIH(ac)/VIL(ac) levels	tDS(base) DDR3-AC175	-	-	ps	
	tDS(base) DDR3-AC150	30	-	ps	
	tDS(base) DDR3-AC160	-	-	ps	
	tDS(base) DDR3-AC135	45	-	ps	
Data hold time to DQS,DQS# reference to VIH(ac)/VIL(ac) levels	tDS(base) DDR3-DC100	65	-	ps	
	tDS(base) DDR3-DC90	75	-	ps	
DQ and DM Input pulsewidth for each input	tDIPW	400	-	ps	

Table 99 DDR3-1333(L) Timing Parameters II

Parameter	Abbreviation	DDR3-1333(L)		Unit	Notes
		Min	Max		
Data Strobe Timing					
DQS,DQS# differential Read Preamble	tRPRE	0.9	Note 19	tCK(avg)	
DQS,DQS# differential Read Postamble	tRPST	0.3	Note 11	tCK(avg)	
DQS,DQS# differential output high time	tDQH	0.4	-	tCK(avg)	
DQS,DQS# differential output low time	tDQL	0.4	-	tCK(avg)	
DQS,DQS# differential Write Preamble	tWPRE	0.9	-	tCK(avg)	
DQS,DQS# differential Write Postamble	tWPST	0.3	-	tCK(avg)	
DQS,DQS# rising edge output access time from rising CK,CK#	tDQSCK	-255	255	ps	

DQS,DQS# low-impedance time(Referenced from RL-1)	tLZ(DQS)	-500	250	ps	
DQS,DQS# high-impedance time(Referenced from RL+BL/2)	tHZ(DQS)	-	250	ps	
DQS,DQS# differential input low pulse width	tDQSL	0.45	0.55	tCK(avg)	
DQS,DQS# differential input high pulse width	tDQSH	0.45	0.55	tCK(avg)	
DQS,DQS# rising edge to CK,CK# rising edge	tDQSS	-0.25	0.25	tCK(avg)	
DQS,DQS# falling edge setup time to CK,CK# rising edge	tDSS	0.2	-	tCK(avg)	
DQS,DQS# falling edge hold time to CK,CK# rising edge	tDHS	0.2	-	tCK(avg)	
Command and Address Timg					
DLL locking time	tDLLK	512	-	nCK	
Internal READ Command to Precharge Command delay	tRTP	max(4nCK,7.5ns)	-		
Delay from start of internal write transaction to interal read command	tWTR	max(4nCK,7.5ns)	-		
Write recovery time	tWR	15	-	ns	
Mode Register Set Command cycle time	tMRD	4	-	nCK	
Mode Register Set Command update delay	tMOD	max(12nCK,15ns)	-		
ACT to internal read or write delay time	tRCD	See Speed Bin			
PRE Command period	tRP				
ACT to ACT or PRE command preiod	tRC				
Active to Precharge command preiod	tRAS				
CAS# to CAS# command delay	tCCD	4	-	nCK	
Auto precharge write recovry + precharge time	tDAL(min)	WR+round(tRP/tCK(avg))		nCK	

Table 100 DDR3-1333(L) Timing Parameters III

Parameter	Abbreviation	DDR3-1333(L)		Unit	Notes
		Min	Max		
Multi-Purpose Regsister Recovery Time	tMPRR	1	-	nCK	
Active to Active command period for 1KB page size	tRRD	max(4nCK,6ns)	-		
Active to Active command period for 2KB page size	tRRD	max(4nCK,7.5ns)	-		
Four activate window for 1KB page size	tFAW	30	-	ns	
Four activate window for 2KB page size	tFAW	45	-	ns	
Command and Address setup time to CK,CK# reference to VIH(ac)/VIL(ac) levels	tIS(Base)DDR3-AC175	65	-	ps	
	tIS(Base)DDR3-AC150	190	-	ns	

	tIS(Base)DDR3-AC160	80	-	ps	
	tIS(Base)DDR3-AC135	205	-	ns	
Command and Address hold time to CK,CK# reference to VIH(ac)/VIL(ac) levels	tIS(Base)DDR3-DC100	140	-	ns	
	tIS(Base)DDR3-DC90	150	-	ns	
Contrl and Address input pulse width each input	tIPW	620	-	ps	
Calibration Timng					
Power up and RESETcalibration time	tZQinit	tZQinitmin:max(512tCK,640ns) tZQinitmax:-		nCK	
Normal operation full calibration time	tZQoper	tZQopermin:max(256tCK,320ns) tZQopermax:-		nCK	
Normal opereation Short calibration time	tZQCS	tZQCSmin:max(64tCK,80ns) tZQCSmax:-		nCK	
Reset Timing					
Exit Reset from CKE high to a valid command	tXRP	max(5nCK, tRFC(min)+10ns)	-		
Self Refresh Timing					
Exit Self Refresh to commands not requiring a Locked DLL	tXS	max(5nCK,tRFC(min)+10ns)	-		
Exit Self Refresh to commands requiring a Locked DLL	tXSDLL	tDLLK(min)	-	nCK	
Minimum CKE low width for Self Refresh entry to Exit timing	tCKSER	tCKE(min)+1 nCK	-		
Valid Clock Requirement after Self Refresh entry (SRE) or Power Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-		
Valid Clock Requirement before Self Refresh exit(SRX) or Power Down Power Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-		

Table 101 DDR3-1333(L) Timing Parameter Set IV

Parameter	Abbreviation	DDR3-1333(L)		Unit	Notes
		Min	Max		
Power Down Timing					
Exit Power Down with DLL on to any valid command: Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK,6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a Locked DLL	tXDLL	max(10nCK,24ns)	-		
CKE minimum pulse width	tCKE	max(3nCK,5.625ns)	-		
Command pass disable delay	tCPDED	1	-	nCK	

Power Down Entry to Exit Timing	tPD	tCK(min)	9*tREFI		
Timing of ACT command to Power Down entry	tACTPDEN	1	-	nCK	
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	nCK	
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK	
Timing of WR command to Power Down entry(BL8OFT,BL8MRS,BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	nCK	
Timing of WRA command to Power Down entry(BL8OFT,BL8MRS,BC4OTF)	tWRPADEN	WL+4+WR+1	-	nCK	
Timing of WR command to Power Down entry(BC4MRS)	tWRPDEN	WL+2+(tWR/tCK(avg))	-	nCK	
Timing of WRA command to Power Down entry(BC4MRS)	tWRPADEN	WL+2+WR+1	-	nCK	
Timing of REF command to Power Down entry	tREFPDEN	1	-	nCK	
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-		
ODT Timing					
ODT turn on Latency	ODTLon	WL-2=CWL+AL-2	-	nCK	
ODT turn offn Latency	ODTloff	WL-2=CWL+AL-2	-	nCK	
ODT high time without write command or with write command and BC4	ODTH4	4	-	nCK	
ODT high time with write command and BL8	ODTH8	6	-	nCK	
Asynchronous RTT turn on delay (Power Down with DLL frozen)	tAONPD	2	8.5	ns	
Asynchronous RTT turn off delay (Power Down with DLL frozen)	tAOFPD	2	8.5	ns	
Down with DLL frozen)					
RTT turn on	tAON	-250	250	ps	
RTT_Nom and RTT_WR turn off time from ODTLoff reference	tAOF	0.3	0.7	tCK(avg)	
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)	

Table 102 DDR3-1333(L) Timing Parameter Set V

Parameter	Abbreviation	DDR3-1333(L)		Unit	Notes
		Min	Max		
Write Leveling Timing					
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	nCK	
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	nCK	
Write Leveling setup time from rising CK,CK# crossing to rising DQS,DQS# crossing	tWLS	195	-	ps	

Write Leveling hold time from rising DQS,DQS# crossing to rising CK,CK# crossing	tCPDED	195	-	ps	
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CK,CK# crossing					
Write leveling output delay	tWLO	0	9	ns	
Write leveling output error	tWLOE	0	2	ns	

Speed Bin (DDR3(L)-1600/1866/2133) Timing Parameters

Table 103 DDR3-1600(L)/1866(L)/2133(L) Timing Parameters I

Parameter	Abbreviation	DDR3-1600(L)		DDR3-1866(L)		DDR3-2133(L)		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock Timng									
Minimum Clock Cycle Time (DLL off mode) off mode)	tCK(DLL_OFF)	8	-	8	-	8	-	ns	
Average Clock Period Period	tCK(avg)	Reference Speed Bin						ps	
Average high pulse width width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Absolute Clock Period Period	tCK(abs)	min:tCK(avg)min+tJIT(per)min max:tCK(avg)max+tJIT(per)max						ps	
Absolute high pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	
Absolute low pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	
Clock Period Jitter	tJIT(per)	-70	70	-60	60	-50	50	ps	
Clock Period Jitter during DLL locking Period	tJIT(per,lck)	-60	60	-50	50	-40	40	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	140		120		100		ps	
Cycle to Cycle Period Jitter during DLL locking Period locking Period	tJIT(cc,lck)	120		100		80		ps	
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	-	-	ps	
Cumulative error across n = 13,14...49,50 cycles cycles	tERR(nper)	tERR(nper)min=(1+0.68ln(n))*tJIT(per)min tERR(nper)max=(1+0.68ln(n))*tJIT(per)max						ps	
Data Timng									

DQS,DQS# to DQ skew, per group, per access	tDQSQ	-	180	-	85	-	75	ps	
DQ output hold time hold time from DQS, DQS#	tQH	0.38	-	0.38	-	0.38	-	tCK(avg)	
DQ low impedance time from CK,CK#	tLZ(DQ)	-450	225	-390	195	-360	180	ps	
DQ high impedance time from CK,CK#	tHZ(DQ)	-	225	-	195	-	180	ps	
Data setup time to DQS,DQS# reference to VIH(ac)/VIL(ac) levels	tDS(base) DDR3-1600(AC175) DDR3-1866/2133 (AC150)	-	-	-	-	-	-	ps	
	tDS(base) DDR3-1600(AC150) DDR3-1866/2133(AC135) (AC135)	10	-	68	-	53	-	ps	
	tDS(base) DDR3-1600(AC135) SR=1V/ns tDS(base) DDR3-1866(AC1130) SR=2V/ns	25	-	70	-	55	-	ps	
Data setup time to DQS, DQS# reference to VIH(ac)/VIL(ac) levels	tDS(base) DDR3-DC100	45	-	70	-	55	-	ps	
	tDS(base) DC90 DDR3-1600(SR=1V/ns) DDR3-1866(SR=2V/ns) 2V/ns)	55	-	75	-	60	-	ps	
DQ and DM Input pulsewidth for each input	tDIPW	360	-	320	-	280	-	ps	

Table 104 DDR3-1600(L)/1866(L)/2133(L) Timing Parameters II

Parameter	Abbreviation	DDR3-1600(L)		DDR3-1866(L)		DDR3-2133(L)		Unit	Notes
		Min	Max	Min	Max	Min	Max		

Data Strobe Timing									
DQS, DQS# differential read preamble Preamble	tRPRE	0.9	Note 19	0.9	Note 19	0.9	Note 19	tCK(avg)	
DQS,DQS# differential Read	tRPST	0.3	Note 11	0.3	Note 11	0.3	Note 11	tCK(avg)	
Postamble									
DQS, DQS# differential output output high time	tDQH	0.4	-	0.4	-	0.4	-	tCK(avg)	
DQS,DQS# differential output low time	tDQL	0.4	-	0.4	-	0.4	-	tCK(avg)	
DQS, DQS# differential write Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK(avg)	
DQS,DQS# differential Write Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK(avg)	
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSK	-255	255	-195	195	-180	180	ps	
DQS, DQS# low-impedance time (referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	ps	
DQS,DQS# high-impedance time(Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	ps	
DQS,DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)	
DQS,DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)	
DQS,DQS# rising edge to CK,CK# rising edge	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK(avg)	
DQS,DQS# falling edge setup Setup time to CK, CK# rising edge	tDSS	0.18	-	0.18	-	0.18	-	tCK(avg)	
DQS, DQS# falling edge hold time time to CK,CK# rising edge	tDHS	0.18	-	0.18	-	0.18	-	tCK(avg)	
Command and Address Timing									
DLL locking time	tDLLK	512	-	512	-	512	-	nCK	
Internal READ Command to Precharge Command delay	tRTP	tRTP(min): max(4nCK, 7.5ns) tRTP(max): -							
Delay from start of internal write transaction to internal read command	tWTR	tWTRmin:max(4nCK,7.5ns) tWTRmax:-							
Write recovery time	tWR	15	-	15	-	15	-	ns	
Mode Register Set Command cycle time	tMRD	4	-	4	-	4	-	nCK	
Mode Register Set Command update delay	tMOD	tMODmin:max(12nCK,15ns) tMODmax:-							

ACT to internal read or write delay time	tRCD	See Speed Bin		
PRE Command period	tRP			
ACT to ACT or PRE command period preiod	tRC			

Active to Precharge command period	tRAS								
CAS# to CAS# command delay	tCCD	4	-	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR+round(tRP/tCK(avg))						nCK	

Table 105 DDR3-1600(L)/1866(L)/2133(L) Timing Parameters III

Parameter	Abbreviation	DDR3-1600(L)		DDR3-1866(L)		DDR3-2133(L)		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	
Active to Active command period for 1KB page size	tRRD	tRRDmin:max(4nCK,6ns) tRRDmax:-							
Active to Active command period for 2KB page size	tRRD	tRRDmin:max(4nCK,7.5ns) tRRDmax:-							
Four activate window for 1KB page size	tFAW	30	-	27	-	25	-	ns	
Four bank activate window for 2KB page size	tFAW	40	-	35	-	35	-	ns	
Command and Address setup time to CK,CK# reference to VIH(ac)/VIL(ac) levels	tIS(Base) DDR3-1600(AC175), DDR3-1866/2133(AC150)	45	-	-	-	-	-	ps	
	tIS(Base) DDR3-1600(AC150), DDR3-1866/2133(AC125)	170	-	150	-	135	-	ns	
	tIS(Base)DDR3-AC160	60	-	-	-	-	-	ps	
	tIS(Base)DDR3-AC135	185	-	65	-	60	-	ps	
	tIS(Base) DDR3 (AC125)	-	-	150	-	135	-	ps	
Command and	tIS(Base)DDR3-DC100	120	-	100	-	95	-	ps	

Address hold time to CK,CK# reference to VIH(ac)/VIL(ac) levels	tIS(Base)DDR3-DC90	130	-	110	-	105	-	ps	
Command and Address input pulse width each input input	tIPW	560	-	535	-	470	-	ps	
Calibration Timng									
Power up and RESET calibration time	tZQinit	tZQinit(min): max(512 tCK, 640 ns); tZQinit(max): -						nCK	
Normal Operation Full calibration time	tZQoper	tZQoper(min): max(256 tCK, 320 ns); tZQoper(max): -						nCK	
Normal operation Short calibration time	tZQCS	tZQCS(min): max(64 tCK, 80 ns); tZQCS(max): -						nCK	
Reset Timing									
Exit Reset from CKE high to a valid command valid command	tXRP	tXRPmin:max(5nCK,tRFC(min))+10ns) tXRPmax:-							
Self Refresh Timing									
Exit Self Refresh to commands not requiring a Locked DLL	tXS	tXSmin:max(5nCK,tRFC(min))+10ns) tXSmax:-							
Exit Self Refresh to commands requiring a Locked DLL	tXSDLL	tXSDLLmin:tDLLK(min) tXSDLLmax:-						nCK	
Minimum CKE low width for Self Refresh entry to Exit timing	tCKSER	tCKSERmin:tCKE(min)+1 nCK tCKSERmax:-							
Valid Clock Requirement after Self Refresh entry (SRE) or Power Down entry (PDE) Entry(PDE)	tCKSRE	tCKSRE min: max(5 nCK, 10 ns); tCKSRE max: -							
Valid Clock	tCKSRX	tCKSRX min: max(5 nCK, 10 ns)							

Requirement before Self Refresh exit (SRX) or Power Down Exit (PDX) or Reset Exit Reset Exit		tCKSRXmax:-		
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Table 106 DDR3-1600(L)/1866(L)/2133(L) Timing Parameters (Table IV)

Parameter	Abbrevia tion	DDR3-1600(L)		DDR3-1866(L)		DDR3-2133(L)		Unit	No tes
		Min	M ax	Min	M ax	Min	M ax		
Power Down Timing									
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL DLL	tXP	tXPmin: max(3nCK, 6ns); tXPmax: -							
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL DLL	tXDLL	tXDLLmin: max(10nCK, 24ns); tXDLLmax: -							
CKE minimum pulsewidth width	tCKE	tCKEmin:max(3nCK,5ns) tCKEmax:-							
Command pass disable delay	tCPDED	1	-	1	-	1	-	nCK	
Power Down Entry to Exit Timing	tPD	tPDmin:tCK(min) tPDmax:9*tREFI							
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	nCK	
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	1	-	nCK	
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8 OTF, BL8 MRS)	tWRPDEN	WL+4+(tWR/tCK(avg)) CK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	

MRS, BC4 OTF)									
Timing of WRA command to Power Down entry (BL8 OTF, BL8 MRS) RS,BC4OTF)	tWRPA DEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	
Timing of WR command to Power Down entry(BC4MRS)	tWRP D EN	WL+2+(tWR/tCK(avg)) CK(avg))	-	WL+2+(tWR/t CK(avg))	-	WL+2+(tWR/t CK(avg))	-	nCK	
Timing of WRA command to Power Down entry(BC4MRS)	tWRPA DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	
Timing of REF command to Power Down entry	tREFP DEN	1	-	1	-	1	-	nCK	
Timing of MRS command to Power Down entry	tMRSP DEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
ODT Timing									
ODT turn on Latency	ODTLo n	WL-2=CWL+AL-2						nCK	
ODT turn offn Latency	ODTLo ff	WL-2=CWL+AL-2						nCK	
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	nCK	
ODT high time with write command and BL8	ODTH8	6	-	6	-	6	-	nCK	
Asynchronous RTT turn on delay (Power Down with DLL frozen)	tAON P	2	8.5	2	8.5	2	8.5	ns	
Asynchronous RTT turn off delay (Power Down with DLL frozen)	tAOF P	2	8.5	2	8.5	2	8.5	ns	
RTT turn on	tAON	-255	255	-195	195	-180	180	ps	

RTT_Nom and RTT_WR turn off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	

Table 107 DDR3-1600(L)/1866(L)/2133(L) Timing Parameters (Table V)

Parameter	Abbreviation	DDR3-1600(L)		DDR3-1866(L)		DDR3-2133(L)		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Leveling Timing									
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	
Write Leveling setup time from rising CK,CK# crossing to rising DQS,DQS# crossing	tWLS	165	-	140	-	125	-	ps	
Write Leveling hold time from rising DQS,DQS# crossing to rising CK,CK# crossing	tCPDED	165	-	140	-	125	-	ps	
Write leveling output delay	tWLO	0	7.5	0	7.5	0	7.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	ns	

Note 1

(Jitter)

Unit "tCK(avg)" indicates the actual tCK(avg) of the input clock under operation. Unit "nCK" indicates one clock cycle of the input clock, counting actual clock edges. For example: tMRD = 4[nCK] means that if a mode register set command is registered at Tm, another mode register set command can be registered at Tm+4, where the minimum of (Tm+4 – Tm) is 4 × tCK(avg) + tERR(4per).

Note 2

These parameters are measured from the signal edge of command/address signals (CKE, CS#, RAS#, CAS#, WE#, ODT, BA0, A0, A1, etc.) to their respective clock signal (CK, CK#) crossing point. The specification values are not affected by the amount of applied clock jitter (i.e., tJIT(per), tJIT(cc), etc.), because setup and hold times are measured relative to the clock signal crossing point that latches the command/address. That is, these parameters shall be met regardless of the presence of clock jitter.

Note 3

These parameters are measured from the data strobe signal (DQS(L/U), DQS#(L/U)) crossing to their corresponding clock signal (CK, CK#) crossing point. The specification values are not affected by the amount of applied clock jitter (i.e., tJIT(per), tJIT(cc), etc.), because the measurement is relative to the clock signal crossing point.

That is, these parameters shall be met regardless of the amount of clock jitter. Note 4

These parameters are measured from the transition edge of data signals (DM(L/U), DQ(L/U)0, DQ) to their respective data strobe signal (DQS(L/U), DQS#(L/U)) crossing point.

Note 5

For these parameters, DDR3(L) SDRAM devices support $tPARAM[nCK] = \text{ROUNDUP}(tPARAM[ns] / tCK(avg)[ns])$, where the number of clock cycles is calculated assuming all input clock jitter specifications are met.

Note 6

When the device operates with input clock jitter, this parameter must be derated based on the actual $tERR(mper)$ value of the input clock, where $2 < m \leq 12$. (Output derating is relative to the SDRAM input clock.)

Note 7

When the device operates with input clock jitter, this parameter must be derated based on the actual $tJIT(per)$ value of the input clock. (Output derating is relative to the SDRAM input clock.)

Timing Parameter Notes

1. The actual value depends on the definition of the measurement level.
2. Commands that require DLL lock: READ (and RAP) are synchronous ODT commands.
3. Maximum value depends on the system.
4. WR programmed in the mode register.
5. Value must be rounded up to the next integer.
6. There is no maximum cycle time limit other than satisfying the refresh interval $tREFI$.
7. For the definition of RTT turn-on time $tAON$, see "Timing Parameters".
8. For the definition of RTT turn-off time $tAOF$, refer to "Timing Parameters".
9. tWR is defined in ns; to calculate $tWRPDEN$, it is necessary to round up tWR/tCK to the next integer.
10. WR is programmed in MR0.
11. The maximum read postamble is bounded by $tDQSCK(min)$ plus $tQSH(min)$ on the left side and $tHZ(DQS)max$ on the right side.
12. Output timing derating is relative to the SDRAM input clock. When the device operates with input clock jitter, this parameter needs to be TBD reduced.
13. Values are valid for RON34 only.
14. Single-ended signal parameters.

15. tREFI depends on TOPER.
16. tIS(base) and tIH(base) values are for 1 V/ns CMD/ADD single-ended slew rate and 2 V/ns CK, CK# differential slew rate. Note that for DQ and DM signals, $VREF(DC) = VREF(DQ)(DC)$. For input-only pins except RESET, $VREF(DC) = VREF(CA)(DC)$.
(DC).
17. tDS(base) and tDH(base) values are specified for 1 V/ns single-ended slew rate for DQ and 2 V/ns differential slew rate for DQS, DQS#. Note that for DQ and DM signals, $VREF(DC) = VREF(DQ)(DC)$. For input-only pins, except RESET#, $VREF(DC) = VREF(CA)(DC)$.
(DC).
18. The start of an internal write transaction is defined as follows:

For BL8 (fixed and dynamic by MRS): the rising clock edge 4 clock cycles after RL. For BC4 (dynamic): the rising clock edge 4 clock cycles after RL.

For BC4 (fixed by MRS): the rising clock edge 2 clock cycles after RL.
19. The maximum preamble is bounded by tLZ(DQS) max on the left and tDQSCK(max) on the right.
20. CKE is allowed to be registered LOW during operations such as row activation, precharge, auto precharge, or refresh, but the power-down IDD specification is not applied until these operations are completed.
21. Although CKE is allowed to be driven LOW after a REFRESH command once tREFPDEN(min) is satisfied, additional timing parameters such as tXPDLL(min) may still be required.
22. This parameter defines the time between the end of an MPR read burst and an MRS to reload MPR or disable MPR function.
23. The ZQCS command can effectively correct the minimum 0.5% (ZQ Correction) of RON and RTT impedance errors within 64 nCK, depending on the maximum sensitivities specified in the Output Driver Voltage and Temperature Sensitivity and ODT Voltage and Temperature Sensitivity tables.
A method for calculating the ZQCS command interval is provided, assuming the SDRAM is subjected to temperature drift rate (Tdriftrate) and voltage drift rate (Vdriftrate) in the application. The interval can be defined by the formula: $ZQ\ Correction / [(TSens \times Tdriftrate) + (VSens \times Vdriftrate)]$.
For example, if $TSens = 1.5\%/^{\circ}C$, $VSens = 0.15\%/mV$, $Tdriftrate = 1\ ^{\circ}C/s$, $Vdriftrate = 15\ mV/s$, then the interval between ZQCS commands is calculated as $0.5 / [(1.5 \times 1) + (0.15 \times 15)] = 0.133\ s \approx 133\ ms$.
24. n = 13 to 50 cycles. This row defines 38 parameters.
25. tCH (abs) is the absolute instantaneous clock high pulse width measured from a rising edge to the next falling edge.
26. tCL (abs) is the absolute instantaneous clock low pulse width measured from a falling edge to the next rising edge.
27. The tIS(base) AC150 specification adds an additional 100 ps derating to the tIS(base) specification to accommodate the lower AC threshold of 150 mV, plus 25 ps to account for reference point change $[(175\ mV - 150\ mV) / (1\ V/ns)]$.
Address/Command Setup, Hold, and Derating

For all input signals, the total required tIS (setup time) and tIH (hold time) are calculated by adding the data sheet tIS(base) and tIH(base)...

values, respectively, with the Δt_{IS} and Δt_{IH} derating values. Example: t_{IS} (total setup time) = $t_{IS}(\text{base}) + \Delta t_{IS}$

The nominal slew rate for Setup (t_{IS}) of a rising signal is defined as the slew rate between the last crossing of $V_{ref}(\text{dc})$ and the first crossing of $V_{IH}(\text{ac})$ min. The nominal slew rate for Setup (t_{IS}) of a falling signal is defined as the slew rate between the last crossing of $V_{ref}(\text{dc})$ and the first crossing of $V_{IL}(\text{ac})$ max. If the actual signal always precedes the nominal slew rate line between the " $V_{ref}(\text{dc})$ to ac region", then the nominal slew rate is used as the derating value. If the actual signal lags the nominal slew rate line between the " $V_{ref}(\text{dc})$ to ac region", then the slew rate of the tangent of the actual signal from the ac level to the dc level is used for the derating value.

The nominal slew rate for Hold (t_{H}) of a rising signal is defined as the slew rate between the last crossing of $V_{IL}(\text{dc})$ max and the first crossing of $V_{ref}(\text{dc})$. The nominal slew rate for Hold (t_{H}) of a falling signal is defined as the slew rate between the last crossing of $V_{IH}(\text{dc})$ min and the first crossing of $V_{ref}(\text{dc})$. If the actual signal always lags the nominal slew rate line between the " dc to $V_{ref}(\text{dc})$ region", then the nominal slew rate is used as the derating value. If the actual signal precedes the nominal slew rate line between the " dc to $V_{ref}(\text{dc})$ region", then the slew rate of the tangent of the actual signal from the dc level to the $V_{ref}(\text{dc})$ level is used for the derating value. For a valid transition, the input signal must remain above/below $V_{IH}/V_{IL}(\text{ac})$ for a certain period. Although for slow slew rates, the total setup time may be negative (i.e., the valid input signal will not have

reached $V_{IH}/V_{IL}(\text{ac})$), but still requires the valid input signal to complete the transition and reach $V_{IH}/V_{IL}(\text{ac})$.

Base values for ADD/CMD setup and hold at 1V/ns

Table 108 Base Values for ADD/CMD Setup and Hold Time

Grade	Abbreviation	Parameter	800	1066	1333	1600	1866	2133	Unit	Notes
DDR3	$t_{IS}(\text{base})\text{AC175}$	$V_{IH}/L(\text{ac})$	200	125	65	45	-	-	ps	1
	$t_{IS}(\text{base})\text{AC150}$	$V_{IH}/L(\text{ac})$	350	275	190	170	-	-	ps	1
	$t_{IS}(\text{base})\text{AC135}$	$V_{IH}/L(\text{ac})$	-	-	-	-	65	60	ps	1
	$t_{IS}(\text{base})\text{AC125}$	$V_{IH}/L(\text{ac})$	-	-	-	-	150	135	ps	1
	$t_{IS}(\text{base})\text{DC100}$	$V_{IH}/L(\text{dc})$	275	200	140	120	100	95	ps	1
DDR3	$t_{IS}(\text{base})\text{AC160}$	$V_{IH}/L(\text{ac})$	215	140	80	60	-	-	ps	1
	$t_{IS}(\text{base})\text{AC135}$	$V_{IH}/L(\text{ac})$	365	290	205	186	65	-	ps	1,2
	$t_{IS}(\text{base})\text{AC125}$	$V_{IH}/L(\text{ac})$	-	-	-	-	150	-	ps	1,3
	$t_{IS}(\text{base})\text{DC90}$	$V_{IH}/L(\text{dc})$	285	210	150	130	110	-	ps	1

Notes:

Note 1: The 1 V/ns address/command slew rate and 2 V/ns differential CK-CK# slew rate reference the AC and DC levels.

Note 2: $t_{IS}(\text{base})\text{AC135}$ specification is adjusted from $t_{IS}(\text{base})\text{AC160}$ specification by adding 125 ps for DDR3-800/1066.

or adding 100 ps derating for DDR3-1333/1600 to accommodate the lower AC threshold of 135 mV and adding 25 ps for the earlier reference point (160 mV – 135 mV)

adds 25 ps.

Note 3: The $t_{IS}(\text{base})\text{AC125}$ specification is adjusted from the $t_{IS}(\text{base})\text{AC135}$ specification by adding a regular 75 ps derating

for DDR3-1866 to accommodate the lower AC threshold of 135 mV and adding an additional 10 ps to account for the earlier reference point $[(135 \text{ mV} - 125 \text{ mV})/1 \text{ V/ns}]$.

Derating Values for DDR3-800/1066/1333/1600 tIS/tIH-AC/DC Based on AC160 Threshold

Table 109 DDR3 AC160 Threshold and Signal Slew Rate Compensation I

		DDR3 AC160 Threshold: VIH(AC)=VREF(DC)+160mV, VIL(AC)=VREF(DC)-160mV															
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate(V/ns)	2	80	45	80	45	80	45	88	53	96	61	104	69	112	79	120	95
	1.5	53	30	53	30	53	30	61	38	69	46	77	54	85	64	93	80
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-1	-3	-1	-3	-1	-3	7	5	15	13	23	21	31	31	39	47
	0.8	-3	-8	-3	-8	-3	-8	5	1	13	9	21	17	29	27	37	43
	0.7	-5	-13	-5	-13	-5	-13	3	-5	11	3	19	11	27	21	35	37
	0.6	-8	-20	-8	-20	-8	-20	0	-12	8	-4	16	4	24	14	32	30
	0.5	-20	-30	-20	-30	-20	-30	-12	-22	-4	-14	4	-6	12	4	20	20
	0.4	-40	-45	-40	-45	-40	-45	-32	-37	-24	-29	-16	-21	-8	-11	0	5

Derating Values for DDR3-800/1066/1333/1600 tIS/tIH-AC/DC Based on AC135 Threshold

Table 110 DDR3 AC135 Threshold and Signal Slew Rate Compensation I

		DDR3 AC135 Threshold ->VIH(AC)=VREF(DC)+135mV,VIL(AC)=VREF(DC)-135mV															
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIH S	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate(V/ns)	2	68	45	68	45	68	45	75	53	84	61	92	69	100	79	108	95
	1.5	45	30	45	30	45	30	53	38	61	46	69	54	77	64	85	80
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-3	2	-3	2	-3	10	5	18	13	26	21	34	31	42	47
	0.8	3	-8	3	-8	3	-8	11	1	19	9	27	17	35	27	43	43
	0.7	6	-13	6	-13	6	-13	14	-5	22	3	30	11	38	21	46	37
	0.6	9	-20	9	-20	9	-20	17	-12	25	-4	33	4	41	14	49	30
	0.5	5	-30	5	-30	5	-30	13	-22	21	-14	29	-6	37	4	45	20
	0.4	-3	-45	-3	-45	-3	-45	6	-37	14	-29	22	-21	30	-11	38	5

Derating Values for DDR3-1866/2133 tIS/tIH-AC/DC Based on AC125 Threshold

Table 111 DDR3 AC125 Threshold and Signal Slew Rate Compensation

		DDR3 AC125 Threshold ->VIH(AC)=VREF(DC)+125mV,VIL(AC)=VREF(DC)-125mV																
		CK, CK# Differential Slew Rate																
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns		
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	
Slew Rate(V/ns)	CMD/ADD	2	63	45	63	45	63	45	71	53	79	61	87	69	95	79	103	95
		1.5	42	30	42	30	42	30	50	38	58	46	66	54	74	64	82	80
		1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50

	0.9	3	-3	3	-3	3	-3	11	5	19	13	27	21	35	31	43	47
	0.8	6	-8	6	-8	6	-8	14	1	22	9	30	17	38	27	46	43
	0.7	10	-13	10	-13	10	-13	18	-5	26	3	34	11	42	21	50	37
	0.6	16	-20	16	-20	16	-20	24	-12	32	4	40	-4	48	14	56	30
	0.5	15	-30	15	-30	15	-30	23	-22	31	-14	39	-6	47	4	55	20
	0.4	13	-45	13	-45	13	-45	21	-37	29	-29	37	-21	45	-11	53	5

Derating Values for DDR3-1866/2133 tIS/tIH-AC/DC Based on AC175 Threshold

Table 112 DDR3 AC175 Threshold and Signal Slew Rate Compensation I

		DDR3 AC175 Threshold ->VIH(AC)=VREF(DC)+175mV,VIL(AC)=VREF(DC)-175mV															
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ADD Slew Rate(V/ns)	2	88	45	88	45	88	45	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
	0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

Derating Values for DDR3-1866/2133 tIS/tIH-AC/DC Based on AC150 Threshold

Table 113 DDR3 AC150 Threshold and Signal Slew Rate Compensation I

		DDR3 AC150 Threshold ->VIH(AC)=VREF(DC)+150mV,VIL(AC)=VREF(DC)-150mV															
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ADD Slew Rate(V/ns)	2	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	24	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	24	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	23	-36	7	-26	15	-10

Derating Values for DDR3-1866/2133 tIS/tIH-AC/DC Based on AC135 Threshold

Table 114 DDR3 AC135 Threshold and Signal Slew Rate Derating II

		DDR3 AC135 Threshold ->VIH(AC)=VREF(DC)+135mV,VIL(AC)=VREF(DC)-135mV															
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	

		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ADD Slew Rate(V/ns)	2	68	50	68	50	68	50	76	58	84	66	92	74	100	84	108	100
	1.5	45	34	45	34	45	34	53	42	61	50	69	58	77	68	85	84
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-4	2	-4	2	-4	10	4	18	12	26	20	34	30	42	46
	0.8	3	-10	3	-10	3	-10	11	-2	19	6	27	14	35	24	43	40
	0.7	6	-16	6	-16	6	-16	14	-8	22	0	30	8	38	18	46	34
	0.6	9	-26	9	-26	9	-26	17	-18	25	-10	33	-2	41	8	49	24
	0.5	5	-40	5	-40	5	-40	13	-32	21	-24	29	-16	37	-6	45	10
	0.4	-3	-60	-3	-60	-3	-60	6	-52	14	-44	22	-36	30	-26	38	-10

Derating Values for DDR3-1866/2133 tIS/tIH-AC/DC Based on AC125 Threshold

Table 115 DDR3 AC125 Threshold and Signal Slew Rate Derating

		DDR3 AC125 Threshold $\rightarrow V_{IH}(AC)=V_{REF}(DC)+125mV, V_{IL}(AC)=V_{REF}(DC)-125mV$															
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ADD Slew Rate(V/ns)	2	63	50	63	50	63	50	71	58	79	66	87	74	95	84	103	100
	1.5	42	34	42	34	42	34	50	42	58	50	66	58	74	68	82	84
	1	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	4	-4	4	-4	4	-4	12	4	20	12	28	20	36	30	44	46
	0.8	6	-10	6	-10	6	-10	14	-2	22	6	30	14	38	24	46	40
	0.7	11	-16	11	-16	11	-16	19	-8	27	0	35	8	43	18	51	34
	0.6	16	-26	16	-26	16	-26	24	-18	32	-10	40	-2	48	8	56	24
	0.5	15	-40	15	-40	15	-40	23	-32	31	-24	39	-16	47	-6	55	10
	0.4	13	-60	13	-60	13	-60	21	-52	29	-44	37	-36	45	-26	53	-10

Time tVAC Required for ADD/CMD Signal to Transition from VIL(ac) to VIH(ac)

Table 116 DDR3 Timing Parameter Requirements

Slew Rate[V/ns]	DDR3				DDR3				Unit
	800/1066/1333/1600		1866/2133		800/1066/1333/1600		1866/2133		
	175 ps	150 ps	135 ps	125 ps	160 ps	135mV[ps]	135mV[ps]	125mV[ps]	
>2	75	175	168	173	200	213	200	205	ps
2	57	170	168	173	200	213	200	205	ps
1.5	50	167	145	152	173	190	178	184	ps
1	38	130	100	110	120	145	133	143	ps
0.9	34	113	85	96	102	130	118	129	ps
0.8	29	93	66	79	80	111	99	111	ps
0.7	22	66	42	56	51	87	75	89	ps
0.6	Note	30	10	27	13	55	43	59	ps
0.5	Note	Note	Note	Note	Note	10	Note	18	ps
<0.5	Note	Note	Note	Note	Note	10	Note	18	ps

Note: Rising input signals shall be at or above VIH(ac) level, and falling input signals shall be at or below VIL(ac) level.

Data Setup, Hold, and Slew Rate Derating

For all input signals, the total tDS (setup time) and tDH (hold time) are calculated by adding the Δt_{DS} and Δt_{DH} derating values to the respective tDS(base) and tDH(base) values from the datasheet.

Example: tDS (total setup time) = tDS(base) + Δt_{DS}

The nominal slew rate for Setup (tDS) of a rising signal is defined as the slew rate between the last crossing of Vref(dc) and the first crossing of VIH(ac)min. The nominal slew rate for Setup (tDS) of a falling signal is defined as the slew rate between the last crossing of Vref(dc) and the first crossing of VIL(ac)max. If the actual signal is always earlier than the nominal slew rate line between the "Vref(dc) to ac region", then the nominal slew rate is used as the derating value. If the actual signal is later than the nominal slew rate line between the "Vref(dc) to ac region", then the slew rate of the tangent from the ac level to the dc level of the actual signal is used for the derating value.

The nominal slew rate for Hold (tDH) of a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of Vref(dc). The nominal slew rate for Hold (tDH) of a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of Vref(dc). If the actual signal is always later than the nominal slew rate line between the "dc level to Vref(dc) region", then the nominal slew rate is used as the derating value. If the actual signal is earlier than the nominal slew rate line between the "dc to Vref(dc) region", then the slew rate of the tangent from the dc level to the Vref(dc) level of the actual signal is used for the derating value.

For a valid transition, the input signal must remain above/below VIH/IL(ac) for a period of time tVAC.

Although for slow slew rates the total setup time may be negative (i.e., the valid input signal will not reach VIH/IL(ac) at the rising clock edge),

the valid input signal is still required to complete the transition and reach

VIH/IL(ac). For slew rates between the values listed in the table below, derating

values may be obtained by linear interpolation. These values are typically not

subject to production test. They are verified by design and characterization.

Derating values for DDR3-800/1066 tDS/tDH-AC/DC based on AC160 threshold levels

Table 117 DDR3 AC160 Threshold Levels and Signal Slew Rate Compensation II

		DDR3 AC160 Threshold ->VIH(AC)=VREF(DC)+160mV,VIL(AC)=VREF(DC)-160mV															
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ADD Slew Rate(V/ns)	2	80	45	80	45	80	45	-	-	-	-	-	-	-	-	-	-
	1.5	53	30	53	30	53	30	61	38	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-1	-3	-1	-3	7	5	15	13	23	21	-	-	-	-
	0.8	-	-	-	-	-3	-8	5	1	13	9	21	17	29	27		
	0.7	-	-	-	-	-	-	3	-5	11	3	19	11	27	21	35	37
	0.6	-	-	-	-	-	-	-	-	8	-4	16	4	24	14	32	90
	0.5	-	-	-	-	-	-	-	-	-	-	4	-6	12	4	20	20

	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-8	-11	0	5
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Derating Values DDR3-800/1066/1333/1600 tDS/tDH-AC/DC Based on AC135 Threshold

Table 118 DDR3 AC135 Threshold and Signal Slew Rate Compensation III

		DDR3 AC135 Threshold ->VIH(AC)=VREF(DC)+135mV,VIL(AC)=VREF(DC)-135mV															
		CK, CK# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ADD Slew Rate(V/ns)	2	45	68	45	68	45	68	-	-	-	-	-	-	-	-	-	-
	1.5	45	30	45	30	45	30	53	38	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-3	2	-3	10	5	18	13	26	21	-	-	-	-
	0.8	-	-	-	-	3	-8	11	1	19	9	27	17	35	27	-	-
	0.7	-	-	-	-	-	-	14	-5	22	3	30	11	38	21	46	37
	0.6	-	-	-	-	-	-	-	-	25	-4	33	4	41	14	49	90
	0.5	-	-	-	-	-	-	-	-	-	-	29	-6	37	4	45	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-11	38	5

Derating values for DDR3-1866/2133 tDS/tDH-AC/DC based on AC130 threshold

Table 119 DDR3 AC135 Threshold and Signal Slew Rate Compensation

		DDR3 AC130 Threshold ->VIH(AC)=VREF(DC)+130mV,VIL(AC)=VREF(DC)-130mV																								
		CK, CK# Differential Slew Rate																								
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns		
		Δt IS	Δt IH	Δt IS	Δt IH	Δt IS	Δt IH	Δt IS	Δt IH	Δt IS	Δt IH	Δt IS	Δt IH	Δt IS	Δt IH	Δt IS	Δt IH	Δt IS	Δt IH	Δt IS	Δt IH	Δt IS	Δt IH	Δt IS	Δt IH	
CMD/ADD Slew Rate(V/ns)	4	33	23	33	23	33	23	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
	3.5	28	19	28	19	28	19	28	19	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
	3	22	15	22	15	22	15	22	15	22	15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
	2.5	-	-	13	9	13	9	13	9	13	0	13	9	-	-	-	-	-	-	-	-	-	-	-	-	
	2	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	
	1.5	-	-	-	-	-	-	-22	-15	-22	-15	-22	-15	-22	-15	-14	-7	-	-	-	-	-	-	-	-	
	1	-	-	-	-	-	-	-	-	-65	-45	-65	-45	-65	-45	-57	-37	-49	-29	-	-	-	-	-	-	
	0.9	-	-	-	-	-	-	-	-	-	-	-62	-48	-62	-48	-54	-40	-46	-32	-38	-24	-	-	-	-	
	0.8	-	-	-	-	-	-	-	-	-	-	-	-	-	-61	-53	-53	-45	-45	-37	-37	-29	-29	-19	-	
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-49	-50	-41	-42	-33	-34	-25	-24	-17	-8
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-37	-49	-29	-41	-21	-31	-13	-15	
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-31	-51	-23	-41	-15	-25	

1.5	50	80	90	70	50	138	90	73	ps
1	38	30	45	25	5	85	45	30	ps
0.9	34	13	30	Note	Note	67	30	16	ps
0.8	29	Note	11	Note	Note	45	11	Note	ps
0.7	Note	Note	Note	-	-	16	-	-	ps
0.6	Note	Note	Note	-	-	-	-	-	ps
0.5	Note	Note	Note	-	-	-	-	-	ps
<0.5	Note	Note	Note	-	-	-	-	-	ps

Note: Rising input signals must be equal to or greater than the VIH(ac) level, and falling input signals must be less than or equal to the VIL(ac) level.